TUTORIALS

Saturday, December 7, 2013
2:45 p.m. – 6:00 p.m.

Lincoln East Room // Lincoln West Room // Monroe Room

Topics Presented at 2:45 – 4:15 p.m.

1. *Nano Electronics – The use of Low-Dimensional Systems for Device Applications,* Joerg Appenzeller, *Purdue University*

   Nano electronics is often associated with the development of devices from novel materials that had not been previously explored in the context of electronic transport, while in fact silicon CMOS technology is a perfect example of a successful nano electronics implementation. This statement brings up the question of what novel nano electronics devices have to offer in order to be useful beyond what silicon can do already today and will be able to do in the future.

   Silicon CMOS technology is clearly "nano" in the sense that in particular the channel length has been scaled down well below the 100nm regime. In order to do so without short channel effects impacting the device characteristics, the dimensions of the dielectric and the silicon body have been steadily decreased. However, there is a limit to how thin a silicon slab can be made before scattering makes the mobility unacceptably small. It is the possibility to achieve excellent transport conditions for certain low-dimensional materials with ultra-thin body thicknesses in the 1nm range that makes them in my mind most beneficial for novel nano electronics applications.

   One-dimensional systems like carbon nanotubes and two-dimensional systems like graphene or di-chalcogenides appear attractive exactly in this context since they allow for the desired electrostatic gate control for ultimately scaled devices with channel lengths in the sub-10nm range without the introduction of severe surface scattering effects. Moreover, the ultimate gate control in these systems allows for novel low power devices like the band-to-band tunneling transistor to become reality.

   In this tutorial I will discuss in particular the potential of two-dimensional materials for future device applications. I will elucidate the impact of various material parameters like the effective mass on the device performance by evaluating the available number of one-dimensional modes for maximum current drive. Moreover, I will discuss in how far the ideal electrostatic gate control in these types of devices can prove useful for low power device applications and various scaling aspects.

2. *Interface Properties for SiC and GaN MOS Devices,* T. Paul Chow, Rensselaer Polytechnic Institute

   Wide bandgap semiconductors, such as SiC and GaN, have many attractive material properties, such as high breakdown field, which make them suitable for power electronic applications. In addition, SiC is one of the few semiconductors which can be thermally oxidized to yield a surface SiO_2 gate oxide, allowing the possibility of power MOSFETs. By contrast, for GaN MOS-gated transistors, gate dielectrics, such as SiO_2, Si_3N_4 or Al_2O_3, must be deposited onto GaN. In this tutorial, I will review the recent status of understanding of interfacial properties of 4H-SiC and 2H-GaN MOS devices and compare them to those of Si MOS devices, focusing their similarities and differences as well as unexpected features.

   Despite the ability to thermally oxidize 4H-SiC, it has been found that the interface state density is far from ideal and highly dependent on the crystallographic orientations as well as crystal polytype. Also, the common practice of 4 to 8^o off angle wafer cut designed for polytype control during epitaxial layer

growth has been found to detrimentally impact the MOS properties. Common silicon MOS process optimization techniques have been found to have mixed results. Hydrogen annealing at 700-800ºC has been found to be effective in minimizing D_{it} on (000-1) (or C-face), but not on commonly used (0001) (or Si-face), 4H-SiC surface. On the other hand, NO annealing at 1150-1300ºC has been shown to significantly reduce inversion electron trapping at the SiO_2 /4H-SiC by introducing positive fixed charges, but at the expense of increased carrier scattering. Many of the common device fabrication processing steps, such as activation of dopant implants and Ohmic contact anneal, have also been found to substantially degrade the inversion electron mobility. The most puzzling feature of 4H-SiC is the sodium contamination of gate oxide has resulted in the highest reported inversion electron field-effect mobility (50% of the projected idea value) but the concomitant threshold voltage instability has rendered the process useless.

It is quite surprising to find the unlike GaAs, 2H-GaN MOS inversion, using deposited SiO_2 layer, can be relatively easy to accomplish but its inversion field-effect mobility is significantly better than the best value reported for that in 4H-SiC. The interface state density, as deduced from C-V measurements, is significantly lower in 2H-GaN than that in 4H-SiC, particularly ear the conduction band edges. Also, the polarity of the interface fixed or trapped charges can be either positive or negative, dependent on the nature of the deposited oxides (Si_2O vs. Al_2O_3). Most of the surface treatments, such as plasma etching, tend to irreversibly degrade the GaN MOS properties.

Finally, it is worth pointing out many of the commonly used MOS characterization techniques, such as C-V, need to be modify for SiC and GaN because the 3X larger energy bandgap when compared to Si. Ultraviolet light illumination, sometimes together with elevated temperatures, during C-V sweeping is necessary to excite electrons from energy states deep within the bandgap for interface state density determination.

3. *Energy Harvesting for Self-Powered Electronic Systems*, Rob van Schaijk R&D Manager Sensors & Energy Harvesters, Holst Centre / IMEC

The emerging trend of self-powered electronic systems has created demand for small energy harvesting systems. System autonomy during its intended lifetime is not reached in case batteries are used due to size limitations and the need to recharge. Micro system technology has enabled the development of energy harvesting at the micro scale. However, in their approximate 15 years of existence, energy harvesting has generated more attention than power and still waiting for the killer application. On top of that the choice of harvesting principle strongly depends on the application. During this tutorial vibration, thermal, photovoltaic and radiofrequency power conversion methods and its possible applications will be presented. An overview of the latest results and remaining challenges will be given with the focus on vibration energy harvester. The real facts and figures of miniature harvesters will be presented. Some of the envisioned applications will be covered with a focus on autonomous TPMS (tire pressure monitoring systems), enabled by vibration energy harvesting. Electrostatic and piezoelectric energy harvesters and their fabrication and implementation will be presented. In case of a successful introduction, this application will pave the road to a whole range of devices powered by energy harvesting.

Lincoln East Room // Lincoln West Room // Monroe Room

Topics Presented at 4:30 – 6:00 p.m.

4. *Tunnel FETs - Beating the 60 mV/Decade Limit*, Erik Lind, EIT, Lund University

   Traditional transistors, such as MOSFETs, operate by electrostatic control of thermionic emission over an energy barrier. This configuration leads to a fundamental limit in the steepness in going from the ON to the OFF state. The rate of turn-off, the so called inverse sub threshold slope is for a thermionic device limited to 60 mV/decade at room temperature. This makes CMOS V_{DD} scaling below 0.5 V difficult without increased off-state leakage or a low on-state current.

   Tunnel Field Effects Transistors (TFET) are an emerging set of devices which are not operating under the principles of thermionic emission. They instead rely on band-to-band tunneling, where the current is controlled by electrostatically changing the tunneling distance. Due to the strong dependence of the tunneling current on the tunneling distance, it is possible to achieve an inverse sub threshold slope (point slope) below 60 mV/decade, while operating at room temperature. This could lead to CMOS-type digital switches operating at V_{DD} below 0.5 V, which can give substantially reduced power consumption as compared with traditional CMOS.

   This tutorial will introduce the basic physics of TFETs and explain how a TFET can operate with swings below the classical limit. The tunneling transmission will be discussed using the WBK approximation and complex band structure. Physical transport phenomena and geometrical effects affecting the device on and off current will be highlighted. I will also show how heterostructure based TFETs can substantially improve the on-current.

   The major difficulties in achieving sub 60mV/decade swings will also be introduced. Here, especially the effects due to interface traps and trap assisted tunneling will be assessed. The source doping level also needs to be considered carefully. Finally, a review of the current state of the art TFETs in various geometries and material system will be performed, as well as comparisons to theoretical modeling.

5. *Atomic-Scale Modeling and Simulations for Nanoelectronics*, Sumeet C. Pandey and Roy Meade, Emerging Memory Group, Process R&D, Micron Technology Inc.

   In order to match the rapid pace of materials evaluation for new technologies, a fundamental modeling framework based on quantum-mechanics that is independent of material-specific parameters and the device-size is of central importance. At present, a bottom-up fully ab initio treatment of realistic emerging memory devices face some stringent computational challenges, therefore, a combination of approaches based on electronic structure, quantum transport, molecular dynamics and Monte Carlo (MC) methods with interatomic potentials, in conjunction with consistent experimental data is the most tractable solution to the needs of simulation of device fabrication and operation. In this tutorial, we address a wide range of theories, computational methods, available implementations, and their application to the field of nanoelectronics related to materials development, process optimization, and device performance and reliability.

   The emphasis of the tutorial is placed on specific applications related to memory- and solar-cells technology-development using various atomistic-modeling techniques. The structural, thermodynamic, and electronic property calculations are discussed within plane-wave density-functional theory (DFT) as implemented in Vienna ab initio Simulation Package (VASP). The examples include: a) structure, phase stability, and defect energetics in crystalline solids and nanostructures using total-energy calculations (ReRAM); b) accurate estimation of electron density of states, band structure, band gaps, and trap levels

in transition-metal oxides with non-local hybrid functional and its comparison with DFT+U (ReRAM); c) determination of work function for Pr0.7Ca0.3MnO3 on ZrO2; d) reaction and diffusion pathways and the associated activation energy barriers using climbing-image nudged elastic band (CI-NEB) method (ReRAM); e) polarization under applied macroscopic fields (FeRAM); nd f) calculation of perpendicular magnetic anisotropy (PMA) using noncollinear
DFT with spin-orbit interaction (SOI) (STT-RAM).

Predictive computations of non-crystalline structures of amorphous/glassy solids in devices and their diffusion properties require large-scale long-time dynamical simulations, hence, this will be treated with ab initio MD along with classical MD simulations using force-fields (FF) employing Large-scale Atomic/Molecular Massively Parallel Simulator (LAMMPS). In addition, the electron transport studies within non-equilibrium Green's function (NEGF) formalism and phase-coherent approximation using Atomistix ToolKit (ATK) will be presented: a) comparing methods for transport modeling (accuracy and tractability): numerical atomic orbitals (NAO) with various functional forms and basis sets, semi-empirical, and tight-binding methods; b) estimating the electrical characteristics for metal-insulator-metal (MIM) devices (ReRAM); c) spin transport in magneto-tunnel junctions (MTJ) and tunneling magneto-resistance (TMR) calculations (STT-RAM); and d) transport in low-dimensional carbon-based devices.

For process-level optimization, modeling at various length and time scales can be realized with application-specific in-house MC and kinetic MC schemes that are combined with DFT, FF, and MD. This is discussed for processes, such as: a) growth mechanism of hydrogenated amorphous silicon thin films during plasma deposition; and b) compositional tuning of quantum dots for optimal optoelectronic function.

6. *3D Chip Stacking,* Mukta Farooq, Systems & Technology Group, IBM

3D chip stacking refers to a vertical stack of chips in which individual chips can communicate with each other through electrical connections. 3D chip stacking has the ability to enhance chip performance by increasing bandwidth, reducing wire delay, and enabling better power management. In true 3D chip stacking, all chips except possibly the topmost chip contain TSVs (Through Silicon Vias). TSVs can be introduced into the silicon CMOS transistor fabrication at a number of points in the manufacturing sequence. Key considerations to determine the optimal introduction point include diameter of the TSV, insulating and conducting materials used in the TSV, and the technology node. TSV fabrication considerations include via etching, insulation, metallization, annealing and capping. The final structure must be evaluated for thermo-mechanical integrity and reliability of TSV structures. Additionally, one must also consider the impact of TSVs on devices.

There are different approaches to achieving 3D chip stacking, including die to die stacking, die to wafer stacking, and wafer to wafer stacking. Another important aspect of 3D chip stacking is the interconnection method and interconnection density used to enable chip to chip communication. Conventional solder connections i.e. C4s, may present issues at very fine pitch requirements. This may necessitate the use of copper columns or copper stud joining, or other methods to enable chip to chip connectivity. In this tutorial, we will review the above concepts and also some of the current literature to understand the unique advantages and challenges of 3D chip stacking.

SHORT COURSE

Challenges of 10nm and 7nm CMOS Technologies

Sunday, December 8, 2013
9:00 a.m. – 5:30 p.m.

Course Organizer: Aaron Thean, IMEC
International Ballroom Center

Driven by multiple-patterning and new device introduction at the 22nm/20nm node, process technology has never been more difficult. With rising complexity and cost, the value proposition of CMOS technology scaling is being questioned again, threatening Moore's law. However, the golden age of mobile computing has only just begun and the demand for advanced software and hardware solutions is clear. Hence, the need for advanced process technologies that deliver to power-performance-density needs remains undisputed. It is important to anticipate the problems and devise process solutions for maximum return-on-investment. With 16nm/14nm in heavy development, this short course will examine the challenges and potential solutions for the next nodes: 10nm and 7nm.

Power-efficient transistors are one of the core components of CMOS technologies. Today, low-V_{dd} operations and variability have become important considerations. In the device lecture we will look at scaling trends and recent understanding on aggressively-scaled device architectures, electrostatics, parasitics, and their trade-offs in device design.

In both the power-performance and circuit density views, interconnect plays a significant role. The industry-wide adoption of local interconnect wiring (sub-M1) alleviates some of the escalating wiring congestion. Continuing the scaling trend puts pressure to achieve low RC in reliable narrow lines. Innovative solutions are needed for barrier layers and metallization. With rising costs due to multiple patterning, the BEOL architecture design becomes a problem that extends well into physical design and system architecture as well. The advanced interconnect lecture will review the various factors in detail.

Central to realizing the technology are patterning, process module development, and their integration. Here is where the factors of cost and complexities are most evident. Since the migration from bulk devices to FinFETs (and Ultra-thin SOI), new process challenges have emerged related to fin formation, gap fill, epitaxy, and so on. A much anticipated inflection in patterning is the readiness of EUV and how it will be integrated with other multiple-patterning schemes for 10nm and 7nm. These topics will be reviewed in the process integration and lithography lectures.

Finally, with emerging technologies such as 3-D ICs, heterogeneous scaling at the system level that complements 2-D CMOS scaling become possible. The final lecture will review the state-of-the-art in the context of 10nm and 7nm CMOS, describing the current state and possible paths forward.

Introduction and Overview
Organizer: Aaron Thean, Director of the Logic Program, IMEC

Device challenges and opportunities for 10nm and below CMOS nodes
Instructor: Frederic Boeuf, Advanced Devices Manager, ST Microelectronics

- CMOS scaling overview – Multimedia convergence
- Power/Performance requirements for 10nm and below
- Basics of device scaling – VDT approach – Bulk, UTTB, MuGFET
- Parasitic capacitance scaling
- High Channel Mobility Materials – Ge/SiGe, III-V
- Super-steep sub-threshold swing devices

Challenges of 10nm & 7nm Advanced Interconnect
Instructor: Zsolt Tokei, Program Director for Nano Interconnects, IMEC

- Introduction to BEOL & MOL interconnect
- R & C scaling trends – Where is the limit?
- Requirements of 10nm & 7nm BEOL features & design rules
- Challenges of metallization (Barrier and Fill)
- Low-k materials
- Multiple patterning options & self-align processing
- BEOL reliability & variability
- Emerging materials and processes (Mn barrier, ELD Cu, SAM, CNTs etc...)

Process Integration Challenges in 10nm CMOS Technology
Instructor: Andy Wei, GLOBALFOUNDRIES

- 10nm Scaling Landscape - Industry Trends, PPC, Device Architecture
- Litho vs. Design Architecture: Optical vs. EUV vs. Schedule
- Contact-Mx Integration - driver for density and yield
- Fin Integration - driver for density and performance
- Alternate Fin Materials - driver for performance
- Process Challenges
- New perspectives on variability
- Looking to 7nm and beyond

Manufacturing, Design, and Test of 2.5D- and 3D-Stacked ICs
Instructor: Paul Franzon, Distinguished Alumni Professor of Electrical and Computer Engineering, North Carolina State University

- 3DIC Motivation
- 3DIC Manufacturing
- 3DIC Design
- 3DIC Test
- Conclusions and Future perspectives

Lithography challenges and EUV readiness for 10nm and beyond
Instructor: Mark Neisser, Resist and Materials Research Manager, Sematech

- Introduction to Lithography and Patterning needs of 10nm and 7nm logic node devices
- Ways to extend multiple pattering
- EUV lithography challenges and status
- Next-Generation Lithography: Directed Self Assembly (DSA) & Nanoimprint etc.

SHORT COURSE

Beyond CMOS: Emerging Materials and Devices

Sunday, December 8, 2013
9:00 a.m. – 5:30 p.m.

Course Organizer: Thomas N. Theis, Semiconductor Research Corp., Durham, NC
International Ballroom East

Innovation in materials and device structures will extend the CMOS digital technology roadmap, but more radical innovation – new device concepts that circumvent the voltage scaling limits of the conventional FET – will be needed to break from the current *status quo* of stagnating system clock speeds and increasingly power-constrained performance. The first presentation in this short course sets the stage for the following presentations by examining the new channel materials and device structures that may extend CMOS technology for the next ten years or more. The following presentation focuses on the most well-known "steep slope" or low-voltage device, the tunneling FET or TFET and the great variety of materials being explored for this device. The next presentation reviews the material properties and the physics of nanomagnetic devices, which promise both low-power operation (in the form of magnetoelectric devices) and non-volatility. The third presentation reviews the rigorous methodology developed in recent years under the Semiconductor Research Corporation's Nanoelectronics Research Initiative (NRI) for comparing the performance potential of devices as diverse as TFETs and various nanomagnetic devices. By highlighting the relative strengths and weaknesses of these emerging devices, this benchmarking research has helped to stimulate further invention. The final talk, on emerging devices for quantum computing, emphasizes the vastness of the research landscape waiting to be explored once we look beyond the conventional FET. Fabrication and characterization of these exploratory quantum devices challenges the limits of today's technology, and mastering those challenges will have profound impacts on conventional computing.

Introduction and Overview
Organizer: Thomas N. Theis, Executive Director, SRC Nanoelectronics Research Initiative

Extending the FET
Instructor: Ken Uchida, Keio University

- Challenges toward the end of the CMOS technology roadmap (scaling issues)
- Advanced device structures (ultra-thin channel, FinFET, nanowire, etc.)
- New channel materials (III-V semiconductors, carbon nanotubes, 2D materials)

Tunnel FETs
Instructor: Adrian M. Ionescu, Ecole Polytechnique Federale de Lausanne

- Introduction: power challenge and energy efficiency
- Principle of operation
- Materials and device structures
- Research prospects and outstanding challenges
- Related "steep slope" device concepts (sub-10mV/decade switches, active gate switching: NEM relays and negative capacitance devices).

Nanomagnetic Devices
Instructor: Rolf Allenspach, IBM Research - Zurich

- Introduction to magnetic materials
- Switching mechanisms (magnetic field switching, STT, voltage-controlled magnetism)
- Some exemplary device concepts
  - Magnetic field-switched devices (i.e. nanomagnetic logic)
  - STT-switched and voltage-switched (magnetoelectric) devices
  - Spin wave devices
- Research prospects and outstanding challenges

Performance Benchmarking Methodology for Emerging Devices
Instructor: Dmitri Nikonov, Intel

- Rigorous methodology for benchmarking disparate device concepts
- Comparative results for devices pursued by the Nanoelectronics Research Initiative

Emerging Devices for Quantum Computing
Instructor: Michelle Simmons, University of New South Wales

- Introduction to quantum computing
- Device requirements for a practical quantum computer
- Survey of devices currently being explored.
- A detailed look at one or two promising device concepts

Plenary Session

Monday, December 9, 9:00 a.m.
International Ballroom Center

Welcome and Awards

General Chair: Tahir Ghani, Intel Corporation

Invited Papers

Technical Program Chair: Howard C.-H. Wang, TSMC, GPDD

1.1 Graphene Future Emerging Technology, Andrea C. Ferrari, University of Cambridge

Disruptive technologies are usually characterised by universal, versatile applications, which change many aspects of our life simultaneously, penetrating every corner of our existence. In order to become disruptive, a new technology needs to offer not incremental, but dramatic, orders of magnitude improvements. Moreover, the more universal the technology, the better chances it has for broad base success. Does graphene have a chance to become the next disruptive technology? Can graphene be the material of the 21th century? Are the properties of graphene so unique to overshadow the unavoidable inconveniences of switching to a new technology, a process usually accompanied by large R&D and capital investments? In spite of the inherent novelty associated with graphene and the lack of maturity of graphene technology, a roadmap can be envisaged, including short-term milestones, and some medium- to long-term targets, intrinsically less detailed, but potentially even more disruptive. This should guide the transition towards a technological platform underpinned by graphene, with opportunities in many fields and benefits to society.

1.2 Heterogeneous 3D Integration – Technology Enabler Toward Future Super-Chips, Mitsumasa Koyanagi, Tohoku University

Various concerns such as higher off-state and sub-threshold leakages, V_T variability, and large signal delay by wiring etc. have emerged in high-density and high-performance LSIs as MOSFET is scaling down toward ten nanometer or less. To solve these issues, various kinds of materials, devices and technologies should be integrated onto a Si substrate. A typical example of such new LSI is a heterogeneous integration of compound semiconductor device, photonic devices and spintronic devices with CMOS. The 3D integration is the key for such heterogeneous integration. We call such heterogeneous 3D LSI a super chip. In a plenary talk, the current status of 3D technology is overviewed and some of the backend interconnect issues caused by 3D integration are discussed. In addition, 3D microprocessor with self-test and self-repair function, 3D image sensor with extremely fast processing speed, and 3D biochip etc. are demonstrated as typical examples of super chip which are fabricated by a nano-assembly and an electrostatic temporary bonding.

1.3 Smart Mobile SoC Driving the Semiconductor Industry: Technology Trend, Challenges and Opportunities, Geoffrey Yeap, Qualcomm

Ever since the advent of iPhone in 2007, there has been an explosive growth in demand for smart mobile devices with increasing processing performance and compelling user experiences. Smart mobile devices have become the new center of the ecosystem and the largest platform in the history of mankind for applications, connectivity and new use cases. Smart mobile SOC has become the most important product driver for the semiconductor industry. It is anticipated that there will be over 3 billion 3/4G connections

by 2016 and a potential 1000x increase in mobile data traffic from 2010 to 2020. In the coming years, mobile devices will offer new services and features, support always-on/always-aware connectivity, and deliver battery life that will provide days of active-use experience. The future of mobile computing is a massive opportunity and challenge.

Power efficiency and cost effectiveness are perhaps the foremost twin challenges. To enable the mobile devices of the future, holistic innovation is absolutely needed starting with mobile SOC architecture partition and optimization, and technology and design co-optimization of individual chips such as modem, application processor, RF transceiver, analog core/codec, and power management ICs. Judicious choices from silicon tech nodes down to backend metal/via layers and RC, number of transistors and their specification, and memory selection are needed to co-optimize the competing requirements of a high speed serial CPU, parallel GPU, modem DSP and always-on circuitry as well as RF transceiver for lower cost and power. Architecture partition and integration is another good example to meet increased system capacity and global demand of increasing number of 4G LTE frequency bands. Cost/power reduction and unique product capability are enabled by RF front end integration of power amplifiers, antenna switches/tuners and power envelope tracker through a cost-effective RF SOI SOI instead of the traditional GaAs. A total RF system can be achieved with eWLP to integrate both RF frontend and transceiver in a single package. Success of a mobile SoC critically requires focus on smart, integrated chipset hardware and software system design.

Session 2: Process and Manufacturing Technology – Germanium & III-V CMOS Device and Integration

Monday, December 9, 1:30 p.m.
International Ballroom West
Co-Chairs: *Carlos Mazure, Soitec*
Tsutomo Tezuka, AIST

1:35 p.m.
2.1 InGaAs MOSFETs for CMOS: Recent Advances in Process Technology (Invited), J.A. Del Alamo, Massachusetts Institute of Technology

InGaAs has recently emerged as the most promising non-Si n-channel material for future nano-scale CMOS. This paper reviews recent advances in key enabling process technology of InGaAs MOSFETs and outlines some of the challenges that need to be overcome before this new device family can become a reality.

2:00 p.m.
2.2 High Electron Mobility Triangular InGaAs-OI nMOSFETs with (111)B Side Surfaces Formed by MOVPE Growth on Narrow Fin Structures, T. Irisawa, M. Oda, K. Ikeda, Y. Moriyama, E. Mieda, W. Jevaswan, T. Maeda, O. Ichikawa*, T. Osada*, M. Hata*, Y. Miyamoto**, T. Tezuka, AIST, *Sumitomo Cemical Ltd., **Tokyo Institute of Technology

We have successfully fabricated triangular InGaAs-OI nMOSFETs with smooth (111)B side surfaces on Si. Triangular shaped channels with bottom width down to 30 nm were formed by MOVPE growth on narrow InGaAs-OI fins. The formed (111)B surface was demonstrated to provide higher mobility compared with reference InGaAs-OI tri-gate (1.9x) as well as bulk (100) InGaAs nMOSFETs (1.6x), which is possibly due to reduced Dit in conduction band and resultant suppressed carrier trapping at the MOS interface. Lower noise and hysteresis in triangular device supported this model. High Ion value of 930 μA/μm at L_g = 300 nm indicates the potential of the triangular InGaAs-OI nMOSFETs for ultra-low power and high performance CMOS applications.

2:25 p.m.
2.3 Reconsideration of Electron Mobility in Ge n-MOSFETs from Ge Substrate Side -Atomically Flat Surface Formation, Layer-by-Layer Oxidation, and Dissolved Oxygen Extraction-, C.H. Lee, T. Nishimura, T.Tabata, C. Lu, W. Zhang, K. Nagashio, A. Toriumi, The University of Tokyo

We clarify wafer-related origins for electron mobility degradation in Ge MOSFETs. High-Ns electron mobility was dramatically improved thanks to (i) atomically flat Ge surface formation, followed by (ii) layer-by-layer oxidation. (iii) Oxygen-related defects in Ge substrates could be another origin of the mobility reduction on Ge wafers. By successfully eliminating these scattering sources, we demonstrate intrinsically high electron and hole mobilities in a wide range of Ns.

2:50 p.m.
2.4 Low D_{it} High-k/$In_{0.53}Ga_{0.47}As$ Gate Stack, with CET Down to 0.73 nm and Thermally Stable Silicide Contact by Suppression of Interfacial Reaction, D. Hassan Zadeh, H. Oomine, K. Kakushima, Y. Kataoka, A. Nishiyama, N. Sugii, H. Wakabayashi, K. Tsutsui, K. Natori, H. Iwai, Tokyo Institute of Technology

Highly scaled InGaAs gate stacks with CET= 0.73 nm, D_{it} as low as 7.0×10^{11} ($eV^{-1}cm^{-2}$) and thermal stability up to 600^{o}C is demonstrated by using La_2O_3 as gate dielectric. A silicide/InGaAs junction with excellent controllability at the interface is also proposed. The scalability, low D_{it}, and thermal stability of La_2O_3/InGaAs combined with robust $NiSi_2$/InGaAs junctions indicate a great potential for future 3D structure technology nodes.

3:15 p.m.
2.5 Oxygen Potential Engineering of Interfacial Layer for Deep Sub-nm EOT High-k Gate Stacks on Ge, C.-H. Lee, C. Lu, T. Tabata, W. Zhang, T. Nishimura, K. Nagashio, A. Toriumi, The University of Tokyo

The interfacial layer (IL) control is a key to achieving deepsub-nm EOT gate stacks with maintaining superior interface properties. We propose the thermodynamically robust IL engineering on Ge (Y_2O_3-doped GeO_2 IL). Based on the understanding, we have demonstrated 0.47-nm-thick EOT on Ge, and the highest electron mobility at high-Ns in Ge n-MOSFETs with sub-nm-thick EOT.

3:40 p.m.
2.6 VLSI Processed InGaAs on Si MOSFETs with Thermally Stable, Self-Aligned Ni-InGaAs Contacts Achieving: Enhanced Drive Current and Pathway Towards a Unified S/D Contact Module, R.T.P. Lee, R.J.W. Hill, W.Y. Loh, R.-H. Baek, S. Deora, K. Matthews, C. Huffman, K. Majumdar, T. Michalak*, C. Borst*, P.Y. Hung, C.-H. Chen**, J.-H. Yum, T.-W. Kim, C.Y. Kang, W-E. Wang, D.-H. Kim***, C. Hobbs, P.D. Kirsch, SEMATECH, *College of Nanoscale Science and Engineering, **TSMC assignee at SEMATECH, ***GLOBALFOUNDRIES assignee at SEMATECH

Parasitic resistance (R_{para}) is a grand challenge to successfully hetero-integrate III-V channels onto Si for CMOS application. Here, we report the first statistical I_{Dsat} comparison for non-self-aligned and self-aligned contacts of $In_{0.53}Ga_{0.47}As$ MOSFETs fabricated on large scale Si substrates with VLSI toolsets. We compare non-self-aligned Mo and self-aligned Ni-InGaAs contacts. Devices with self-aligned contacts exhibit a 25% enhancement in I_{Dsat} over devices with non-self-aligned contacts largely due to the 27% reduction in R_{para}. We have also extended the thermal stability of Ni-InGaAs to 500 ^{o}C (highest reported) enabling it to be compatible with BEOL processes. The impact of the Ni-InGaAs process module on tool contamination is discussed. These results are significant to establish a pathway towards a unified Ni-based S/D contact module for Si/(Si)Ge/III-V co-integration on VLSI platforms.

4:05 p.m.
2.7 Self-Aligned III-V MOSFETs: Towards A CMOS Compatible and Manufacturable Technology Solution, Y. Sun, A. Majumdar, C. Cheng, Y. Kim, U. Rana, R. Martin, R. Bruce, K. Shiu, Y. Zhu, D. Farmer, M. Hopstaken, E. Joseph, J. de Souza, M. Frank, S. Cheng, M. Kobayashi, D. Sadana, D. Park, E. Leobandung, IBM TJ Watson Research Center

We demonstrate self-aligned fully-depleted III-V MOSFETs using CMOS-compatible device structures and manufacturable process flows. Processes with good manufacturability and scalability, such as, gate definition and spacer formation using RIE, and formation of self-aligned source/drain extensions (SDE) and self-aligned raised source/drain (RSD), have been established on III-Vs. We demonstrate short-channel devices down to gate length LG = 30 nm. Our best short-channel devices exhibit peak saturation transconductance G_{MSAT} = 1140 µS/µm at L_G = 60 nm and supply voltage V_{DD} = 0.5 V.

4:30 p.m.
2.8 Co-Integration of InGaAs n- and SiGe p-MOSFETs into Digital CMOS Circuits Using Hybrid Dual-Channel ETXOI Substrates, L. Czornomaz, N. Daix, K. Cheng*, D. Caimi, C. Rossel, K. Lister, M. Sousa, J. Fompeyrine, IBM Zurich Research Laboratory, *IBM

We demonstrate for the first time a dense co-integration of co-planar nano-scaled SiGe p-FETs and InGaAs n-FETs. This result is based on hybrid substrates containing extremely-thin SiGe and InGaAs layers on insulators (ETXOI). We first show that such hybrid substrates can be fabricated by direct wafer bonding with stacked high-mobility layers thinner than 8nm. A process flow is presented that allows us to fabricate n- and p-channel field effect transistors with ultra-thin body and BOX (UTBB-FET) on the same wafer. Gate lengths down to 40nm produced at sub-µm half-pitch are achieved. Working CMOS inverters are obtained using a common front-end which confirms the viability of this integration scheme for hybrid high-mobility dual-channel CMOS. We also highlight that back-biasing technique for Vt tuning can still be used despite the dual-channel structure, as implemented in standard ETSOI circuits.

Session 3: Memory Technology – MRAM and NAND
Monday, December 9, 1:30 p.m.
International Ballroom Center
Co-Chairs: Tetsuo Endoh, Tohoku University
Toshitake Yaegashi, Toshiba Corp.

1:35 p.m.
3.1 Future Prospects of MRAM Technologies (Invited), S. Yuasa, A. Fukushima, K. Yakushiji, T. Nozaki, M. Konoto, H. Maehara, H. Kubota, T. Taniguchi, H. Imamura, K. Ando, Y. Shiota*, F. Bonell*, Y. Suzuki*, National Institute of Advanced Industrial Science and Technology (AIST), *Osaka University

This paper describes a review and future prospects of tunnel magnetoresistance (TMR) effect in magnetic tunnel junctions (MTJs) and spin manipulation technologies such as spin-transfer torque (STT) for magnetoresistive random access memory (MRAM). Major challenges for ultrahigh-density MRAM and novel devices related to MRAM are discussed.

2:00 p.m.
3.2 Comprehensive Study of CoFeB-MgO Magnetic Tunnel Junction Characteristics with Single- and Double-Interface Scaling Down to 1X nm, H. Sato, T. Yamamoto, M. Yamanouchi, S. Ikeda, S. Fukami, K. Kinoshita, F. Matsukura, N.Kasai, H. Ohno, Tohoku University

We study characteristics of CoFeB-MgO magnetic tunnel junction with perpendicular easy-axis (p-MTJ) at a reduced dimension down to 1X nm fabricated by hard-mask process. CoFeB-MgO p-MTJ with double-interface shows higher thermal stability down to 1X nm than that with single-interface.

2:25 p.m.
3.3 Highly Manufacturable Multi-Level Perpendicular MTJ with a Single Top-Pinned Layer and Multiple Barrier/Free Layers, K. Tsunoda, M. Aoki, H. Noshiro, T. Takenaga, C. Yoshida, Y. Yamazaki, A. Takahashi, Y. Iba, A. Hatada, M. Nakabayashi, T. Sugii, Low-power Electronics Association & Project (LEAP)

This paper first reports a novel and highly manufacturable multi-level perpendicular magnetic tunnel junction (p-MTJ) with a single top-pinned layer and multiple barrier/free layers. In the proposed p-MTJ structure, all tunnel barriers and free layers lie under the thick pinned layer, which enables good resistance control and large coercivity (Hc) due to the effect of small film roughness. We have also developed a new CoFeB-based free layer and writing scheme to control the stray field and spin-transfer torque (STT). As a result, stable and well-separated four resistance states were demonstrated in resistance-voltage curves with a 65 nm top-pinned p-MTJ.

2:50 p.m.
3.4 Demonstration of Zero-Offset Field Operation for Top-Pinned MTJ with Synthetic Antiferromagnetic Free Layers, C. Yoshida, T. Takenaga, Y. Iba, Y. Yamazaki, H. Uehara, H. Noshiro, K. Tsunoda, A. Hatada, M. Nakabayashi, A. Takahashi, M. Aoki, T. Sugii, Low-power Electronics Association & Project (LEAP)

We have designed and demonstrated a top-pinned magnetic tunnel junction (MTJ) with synthetic antiferromagnetic (SAF) free layer which eliminate the offset field. The key SAF structure was designed based on a prediction deduced from micromagnetic simulations. As a result, fabricated MTJ with SAF free layer exhibited stable switching without application of an external field.

3:15 p.m.
3.5 20-nm Magnetic Domain Wall Motion Memory with Ultralow-Power Operation, S. Fukami, M. Yamanouchi, K.-J. Kim*, T. Suzuki**, N. Sakimura***, D. Chiba*, S. Ikeda, T. Sugibayashi***, N. Kasai, T. Ono*, H. Ohno, Tohoku University, *Kyoto University, **Renesas Electronics Corporation, ***NEC Corporation

We confirmed scalability of magnetic domain wall motion memory devices at small dimensions down to 20 nm. It is found that write current and time are scaled along with device size while sufficient thermal stability and low error rate are maintained. As a result, ultralow-power and reliable operation is possible.

3:40 p.m.
3.6 Highly Reliable M1X MLC NAND Flash Memory Cell with Novel Active Air-Gap and p+Poly Process Integration Technologies, J. Seo, K. Han, T. Youn, H.-E. Heo, S. Jang, J. Kim, H. Yoo, J. Hwang, C. Yang, H. Lee, B. Kim, E. Choi, K. Noh, B. Lee, B. Lee, H. Jang, S. Park, K. Ahn, S. Lee, J. Kim, S. Lee, SK hynix Inc.

Middle-1X nm MLC NAND (M1X) flash cell is intensively characterized with respect to reliability and manufacturability. For the first time, the novel active air-gap technology is applied to alleviate the drop of channel boosting potential of program inhibition mode, BL-BL interference is reduced to our 2y nm node level by this novel integration technology. Furthermore, it also relaxes the effect of process variation like EFH (Effective Field oxide Height) on cell Vt distribution. Better endurance and retention characteristics can be obtained by p+ doped poly gate. By optimization of active air-gap profile and poly doping level,

M1X nm MLC NAND flash memory has been successfully implemented with superior manufacturability and acceptable reliability.

4:05 p.m.
3.7 A Novel Dual-Channel 3D NAND Flash Featuring Both N-Channel and P-Channel NAND Characteristics for Bit-Alterable Flash Memory and A New Opportunity in Sensing the Stored Charge in the WL Space, H.-T. Lue, P.-Y. Du, W.-C. Chen, T.-H. Yeh, K.-P. Chang, Y.-H. Hsiao, Y.-H. Shih, C.-H. Hung, C.-Y. Lu, Macronix International Co., Ltd

This work proposes a novel dual-channel 3D NAND Flash that exhibits both n-channel and p-channel NAND characteristics. The NAND is junction-free without dopant inside the array. Unlike the conventional 3D NAND, the drain side near SSL is N+ doped junction, while source side near GSL is P+ junction. A positive pass-gate read voltage (Vpass,r) induces n-type virtual source/drain for the center WL's, giving an n-channel behavior. On the other hand, a negative Vpass,r induces p-type virtual source/drain, giving the p-channel behavior. Both n- and p-channel reads perform excellent Id-Vg characteristics with very small leakage current. The advantage of this device is that the carrier source of both +FN programming and –FN erasing can be readily provided by either N+ drain or P+ source, respectively, without waiting for the GIDL generated minority carrier for the floating-body 3D NAND. This gives a much faster +/- FN speed than conventional 3D NAND. Moreover, both +FN and –FN can find suitable inhibit method, enabling a novel bit-alterable Flash memory. For the first time we can successfully compare two sensing methods (n- and p-channel read) and identify the trapped charge in the space between WL's. This not only provides characterization of charge lateral profile but also a new opportunity to create another storage node (WL space) inside the array.

4:30 p.m.
3.8 Channel-Stacked NAND Flash Memory with Layer Selection by Multi-level Operation (LSM), W. Kim, Y. Kim, S. Park, J. Seo, S. Lee, J-H. Lee, B-G. Park, Seoul National University

A novel channel stacked NAND flash memory architecture based on layer selection by multi-level operation (LSM) is proposed, fabricated, and characterized. LSM operation scheme and its advantages are studied, and simulation is performed to verify the operation scheme. Electrical characteristics of fabricated array show that 4 layers are clearly distinguished by multi-level operation of 2 string select lines. The proposed architecture can be a promising solution to achieve ultra-high density data storage.

Session 4: Nano Device Technology – Steep Slope Devices
Monday, December 9, 1:30 p.m.
International Ballroom East
Co-Chairs: Elena Gnani, University of Bologna
Dong-Won Kim, Samsung

1:35 p.m.
4.1 Integration of III-V Nanowires on Si: From High-Performance Vertical FET to Steep-Slope Switch (Invited), K. Tomioka, M. Yoshimura, E. Nakai, F. Ishizaka, T. Fukui, Hokkaido University

We present recent progress in integration of vertical III-V nanowire-channels on Si by selective-area epitaxy, and demonstration of high-performance III-V vertical FETs with thin EOT (< 1 nm) as well as steep subthreshold-slope switch using III-V nanowire/Si heterojunction.

2:00 p.m.

4.2 A New Complementary Hetero-Junction Vertical Tunnel-FET Integration Scheme, R. Rooyackers, A. Vandooren, A. Verhulst, A. Walke, K. Devriendt, S. Locorotondo, M. Demand, G. Bryce, R. Loo, A. Hikavyy, T. Vandeweyer, C. Huyghebaert, N. Collaert, A. Thean, imec

This paper presents a new integration scheme for complementary hetero-junction vertical Tunnel FETs (VTFETs), whereby a sacrificial source layer is used during the device fabrication and replaced by the final hetero-source materials, respectively for n- or p-TFETs, thereby minimizing the thermal budget applied to the source junctions. With the demonstration of this source-replacement-last module for a vertical Ge hetero-junction n-TFET, we show that it is possible to grow highly doped hetero-junctions on a Si channel with steep doping profiles and without damaging the high-κ gate-dielectric interface. This scheme allows for the integration of complementary low-bandgap materials on a Si platform providing high on-currents combined with the Si channel based low off-currents.

2:25 p.m.
4.3 Heterojunction TFET Scaling and Resonant-TFET for Steep Subthreshold Slope at sub-9nm Gate-Length, U. Avci, I. Young, Intel Corp.

The Tunneling Field Effect Transistor (TFET) is of interest for future low-power technologies due to its steep subthreshold-slope (SS). In addition to understanding TFET prospects for future technology nodes, we also need to assess if it enables continued scaling required for increasing transistor density. GaSb/InAs heterojunction TFET (Het-j TFET) is one of the leading TFET options due to its high drive-current. In this paper, double-gate (DG) and nanowire (NW) Het-j TFET is atomisticly modeled and compared to MOSFET down to Lg=9nm, i.e. ITRS 2022 node. To achieve TFET characteristics superior to MOSFET, DG body has to be extremely thin, so NW TFET is preferred due to more relaxed thickness and better characteristics. Scaling roadmap shows Het-j TFET requires a 3nm-NW at Lg=9nm with an I_{dsat} advantage over MOSFET for Vdd<0.4V. A new device – the Resonant-TFET (R-TFET), is proposed, with average SS~25mV/dec and 100x I_{dsat} advantage over MOSFET at Vdd=0.27V, thus enabling the scaling of tunneling transistors to sub-9nm gate-lengths.

2:50 p.m.
4.4 Demonstration of Improved Transient Response of Inverters with Steep Slope Strained Si NW TFETs by Reduction of TAT with Pulsed I-V and NW Scaling, L. Knoll, Q. Zhao, A. Nichau, S. Richter, G. Luong, S. Trellenkamp, A. Schäfer, L. Selmi*, K. Bourdelle**, S. Mantl, Forschungszentrum Jülich, *University of Udine, **SOITEC

We present high Ion (64μA/μm) sSi nanowire TFETs. Pulsed I-V TFET characterization shows small SS and a record I_{60} of $1X10^{-2}$μA/μm due to TAT suppression. Scaling the nanowire improves SS and Ion. Transient analysis of TFET inverter demonstrates for the first time that device scaling yields to faster time response.

3:15 p.m.
4.5 Ferroelectric Negative Capacitance Hetero-Tunnel Field-Effect-Transistors with Internal Voltage Amplification, M.H. Lee, J.-C. Lin, Y.-T. Wei, C.-W. Chen*, H.-K. Zhuang, M. Tang**, National Taiwan Normal University, *Cheng Kung University, **PTEK Technology Co., Ltd

The ferroelectric negative capacitance (NC) hetero-tunnel FET is fabricated for the first time, demonstrating the significant improvement in subthreshold swing (~double slope) and peak gm (118% enhancement) due to the internal voltage amplification. The peak gm enhancement at small VDS (-0.1V) indicates the intrinsic benefit by NC without lateral bias. The new concept of coupling the ferroelectric polarization is proposed and synergistically contributes to the performance for future applications of steep subthreshold slope devices.

3:40 p.m.
4.6 Silicon Carbide (SiC) Nanoelectromechanical Switches and Logic Gates with Long Cycles and Robust Performance in Ambient Air and at High Temperature, T. He, R. Yang, V. Ranganathan, S. Rajgopal, M.A. Tupta*, S. Bhunia, M. Mehregany, P.X.-L. Feng, Case Western Reserve University, *Keithley Instruments

We report demonstration of nanoelectromechanical contact-mode switches and logic gates with high performance, enabled by silicon carbide (SiC) nanocantilevers. Our study focus on nanocantilevers at very small scale (in contrast to recent MEMS switches): thicknesses, widths and switching gaps are mostly ~200nm or smaller. Our device motional volume is only ~1um^3, ~1000 to 10000 times smaller than recent MEMS switches that offer long cycles of operations. For the first time, we show that in ambient air, these nanoscale SiC NEMS switches with nanocontacts have switched over 10^7 to 10^{10} cycles without failure, and the testing have been performed over days (device still alive after this). We also show robust mechanical switching events measured at very high temperature (T=500C). Amongst all nanoscale mechanical switches reported lately, we emphasize that our achieved nanodevice lifetimes are to date the best results reported; most of other similar NEMS devices merely operate a few times before failure.

4:05 p.m.
4.7 Quantum Transport Simulations on the Feasibility of the Bilayer PseudoSpin Field Effect Transistor (BiSFET), X. Mou, L. Register, S. Banerjee, The University of Texas at Austin

The feasibility of the Bilayer pseudoSpin Field-Effect Transistor (BiSFET) concept is illustrated in this work using quantum transport simulations, by showing the condensate-assisted high conductance between two oppositely-charged graphene layers and the sub-kBT critical voltage for ON/OFF switching, supporting the proposed ultra-low power consumption which makes BiSFET a "beyond-CMOS" candidate.

Session 5: Modeling and Simulation – Simulation of Nanodevices
Monday, December 9, 1:30 p.m.
Georgetown Room
Co-Chairs: Hiroshi Takeda, Renesas Electronics Corporation
Christoph Jungemann, RWTH Aachen University

1:35 p.m.
5.1 Nano-Device Simulation from an Atomistic View (Invited), N. Mori, G. Mil'nikov, H. Minari, Y. Kamakura, T. Zushi**, T. Watanabe**, M. Uematsu, K. Itoh*, S. Uno*, H. Tsuchiya*, Osaka University, *JST CREST, **Waseda University

We use the non-equilibrium Green's function calculations combined with the R-matrix theory and/or empirical tight-binding method to study the device variability due to discrete dopants and atomic disorder in silicon nanowire field-effect-transistors.

2:00 p.m.
5.2 Surface Roughness Limited Mobility Modeling in Ultra-Thin SOI and Quantum Well III-V MOSFETs, D. Lizzit, D. Esseni, P. Palestri, L. Selmi, DIEGM - Università degli Studi di Udine

This paper presents a new model for surface roughness mobility accounting for the wave-function oxide penetration and can naturally deal with Hetero-Structure. Calibration with experiments in Si MOSFETs

results in a r.m.s. value of the SR spectrum in close agreement with AFM and TEM measurements and for small Tw in III-V UTB MOSFETs we predict a weaker degradation than Tw^6.

2:25 p.m.
5.3 Comprehensive Layout and Process Optimization Study of Si and III-V Technology for sub-7nm Node, C.Y. Kang, R.H. Baek, T.W. Kim, D. Ko, D.H. Kim, T. Michalak*, C. Borst*, D. Veksler, G. Bersuker, R. Hill, C. Hobbs, P.D. Kirsch, SEMATECH, *College of Nanoscale Science and Engineering

In this work, we report III-V device/circuit performance and their variability for various design and process parameters using analytical MC simulation. III-V device compact/BSIM models are developed including geometry dependent parasitic RC. We identify key process parameter for III-V device process development, such as Nit target. Also we present a pathway to improve device & circuit performance at a given FinFET layout.

2:50 p.m.
5.4 Design Options for Hetero-Junction Tunnel FETs with High on Current and Steep Sub-VT Slope, S. Brocard, M.G. Pala, D. Esseni*, IMEP-LAHC, *DIEGM-IUNET

This work presents a systematic design study of nanowire TFETs at LG=17nm employing a 3D Poisson-NEGF solver based on a 8x8 k.p Hamiltonian and including phonon scattering. In particular: (a) we revisit the design of GaSb-InAs based H-TFETs showing that this system is unlikely to yield a broken bangap profile at the very narrow features necessary for a good SS value; (b) we propose new design options for H-TFETs, relying on the use of strain and of a graded molar fraction x in Al(x)Ga(1−x)Sb, which improves remarkably Ion preserving good SS; (c) we show that even not too large densities of interface defects can hinder and frustrate any design strategy aiming at SS values below 60mV/dec.

3:15 p.m.
5.5 A Unified Charge-Current Compact Model for Ambipolar Operation in Quasi-Ballistic Graphene Transistors: Experimental Verification and Circuit-Analysis Demonstration, S. Rakheja, H. Wang, T. Palacios, I. Meric*, K. Shepard*, D. Antoniadis, Massachusetts Institute of Technology (MIT), *Columbia University

This paper presents an alternate compact virtual source (VS) model for carrier transport in quasi-ballistic graphene transistors. The VS model has only a limited number of input parameters that have a physical meaning and can be easily extracted from device characterization. The contribution of the paper is three-fold. First, a new compact VS model for carrier transport in quasi-ballistic GFETs valid in both unipolar and ambipolar regimes is proposed. The model includes self-consistent intrinsic charge/capacitance descriptions extending from DD to the ballistic regime, where gradual channel approximation (GCA) fails. This formulation also allows the model to be easily extended to bi-layer graphene. Second, the model is calibrated against DC and S-parameter measurements of GFETs. Finally, the model is used to simulate the dynamic response of graphene ambipolar frequency multipliers, which demonstrates the model capability for circuit-level simulations.

3:40 p.m.
5.6 Dependence of Intrinsic Performance of Transition Metal Dichalcogenide Transistors on Materials and Number of Layers at the 5 nm Channel-Length Limit, V. Mishra, S. Smith, K. Ganapathi, S. Salahuddin, University of California, Berkeley

Material properties derived from first-principles are used in ballistic quantum transport calculations to investigate the optimal performance of ultimately scaled transition metal dichalcogenide FETs for four

materials and 1-5 layers. Large bandgaps and effective masses result in excellent switching performance at 5 nm gate lengths, thus showing potential for low-power applications.

4:05 p.m.
5.7 Analysis of Dopant Diffusion and Defects in Fin Structure Using an Atomistic Kinetic Monte Carlo Approach, T. Noda, A.K. Kambham*, C. Vrancken*, A. Thean*, N. Horiguchi*, W. Vandervorst*, Panasonic Corporation, *IMEC

An analysis of dopant diffusion and defects in Fin structure using an atomistic lattice kinetic Monte Carlo (KMC) approach are shown. Atomistic KMC simulations are compared with 3D methodology of Atom Probe Tomography (APT). Atomistic dopant distribution in 3D-Fin structure is shown. KMC simulation shows that implant temperature has an impact on amorphization and residual defects and dopant-defect complexes are formed at top-of-Fin and edge-of-Fin-side after SPER.

Session 6: Power and Compound Semiconductor Devices - Power Devices
Monday, December 9, 1:30 p.m.
Jefferson Room
Co-Chairs: Mikael Östling, KTH Royal Institute of Technology
Subramanian Arulkumaran, Nanyang Technological University

1:35 p.m.
6.1 Techniques Towards GaN Power Transistors with Improved High Voltage Dynamic Switching Properties (Invited), J. Würfl, O. Hilt, E. Bahat-Treidel, R. Zhytnytska, P. Kotara, F. Brunner, O. Krueger, M. Weyers, Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik

Current limitations of GaN power devices in terms of dynamic switching are analyzed and techniques towards improving fast high voltage switching are proposed. Normally-off and normally-on GaN transistors are presented that show a dynamic on-state resistance increase of only a factor of 2.5 after switching at 500 V drain bias.

2:00 p.m.
6.2 Total Current Collapse in High-Voltage GaN MIS-HEMTs Induced by Zener Trapping, D. Jin, J. Joh*, S. Krishnan*, N. Tipirneni*, S. Pendharkar*, J. del Alamo, Massachusetts Institute of Technology, *Texas Instruments

We investigate current collapse in GaN MIS-HEMTs for >600 V operation. We observe extreme trapping in the OFF-state leading to total current collapse. We attribute this to high-field tunneling-induced electron trapping ("Zener trapping"). This finding gives urgency to defect control during epitaxial-growth and appropriate field plate structures for high-voltage MIS-HEMTs.

2:25 p.m.
6.3 Mapping of Interface Traps in High-Performance Al_2O_3/AlGaN/GaN MIS-Heterostructures Using Frequency- and Temperature-Dependent C-V Techniques, S. Yang, Z. Tang, K. Wong*, Y. Lin*, Y. Lu, S. Huang, K.J. Chen, Hong Kong University of Science and Technology, *TSMC, Analog/Power & Specialty Technology Division

With an in-situ low-damage native oxide removal process and the formation of a monocrystal-like nitridation inter-layer(NIL), a high-quality Al_2O_3/III-N interface has been obtained in the Al_2O_3(NIL)/AlGaN/GaN MIS devices, delivering C-V characteristics with small frequency dispersion. C-V based techniques have been developed to map the interface traps at the dielectric/III-N interface.

2:50 p.m.

6.4 Monolithically Integrated 600-V E/D-Mode SiNx/AlGaN/GaN MIS-HEMTs and Their Applications in Low-Standby-Power Start-Up Circuit for Switched-Mode Power Supplies, Z. Tang, Q. Jiang, S. Huang*, Y. Lu, S. Yang, C. Liu, X. Tang, S. Liu, B. Li, K. J. Chen, The Hong Kong University of Science and Technology, *Chinese Academy of Sciences

We have experimentally demonstrated monolithically integrated 600-V enhancement-/depletion-mode (E/D-mode) SiNx/AlGaN/GaN MIS-HEMTs featuring high drive current, low OFF-state leakage, high OFF-state breakdown voltage, low ON-resistance and low current collapse. By employing the monolithically integrated E/D-mode MIS-HEMTs, high-voltage low-standby-power start-up circuit for off-line switched-mode power supplies has been realized.

3:15 p.m.

6.5 Remarkable Advances in SiC Power Device Technology for Ultra High Power Systems (Invited), M. Imaizumi, S. Hasegawa, H. Sumitani, M. Iwasaki, S. Hino, T. Watanabe, K. Hamada, N. Miura, S. Nakata, S. Yamakawa, Mitsubishi Electric Corporation

This paper reports our recent results on high voltage and large current SiC power devices, SBDs and MOSFETs, and power modules for high power applications. The merits brought by SiC power devices for a railcar traction inverter system and the reliability of SiC-MOSFETs are also presented.

3:40 p.m.

6.6 Low V_f and Highly Reliable 16 kV Ultrahigh Voltage SiC Flip-Type n-Channel Implantation and Epitaxial IGBT, Y. Yonezawa, T. Mizushima, K. Takenaka, H. Fujisawa, T. Kato, S. Harada, Y. Tanaka, M. Okamoto, Y. Makifuchi, T. Araoka, T. Tsutsumi, M. Yoshikawa, N. Oose, D. Okamto, M. Sometani, N. Kumagai, M. Takei, M. Miyajima, H. Kimura, A. Otsuki*, M. Harashima**, Y. Sano**, E. Morisaki**, K. Fukuda, H. Okumura, T. Kimoto***, National Institute of Advanced Industrial Science and Technology, AIST, *Fuji Electric Co., Ltd., **Tokyo Electron Yamanashi Limited, ***Department of Electronic Science & Engineering

Flip-type n-channel implantation and epitaxial (IE)-IGBT on 4H-SiC carbon face was investigated. IEMOSFET as a MOSFET structure and original wet gate oxidation method were employed, The ultrahigh 16kV blocking voltage, the extremely low V_f(5V@100A/cm^2) ,Vth instability(0.4V) and good temperature stability are achieved, which is useful for Smart Grid system.

4:05 p.m.

6.7 The Safe Operating Volume as a General Measure for the Operating Limits of LDMOS Transistors, A. Ferrara, P.G. Steeneken*, A. Heringa*, B.K. Boksteen, M. Swanenberg*, A.J. Scholten*, L. van Dijk*, J. Schmitz, R.J.E. Hueting, University of Twente, *NXP Semiconductors

The concept of the safe operating area (SOA) is extended to a safe operating volume (SOV) by adding the junction temperature as a third dimensional parameter in the characterization of LDMOS transistors. It is shown that the SOV is almost independent of pulse time, ambient temperature, and device area for LDMOS devices of identical cross-section.

Session 7: Characterization, Reliability, and Yield – Novel Technology Characterization

Monday, December 9, 1:30 p.m.

Lincoln Room

Co-Chairs: Francesco Driussi, Università degli Studi di Udine
Ben Kaczer, imec

1:35 p.m.

7.1 Revisiting the Silicon-Lattice in the High-Density 3D-LSIs _ in the Perspective of Device Reliability, M. Murugesan, T. Fukushima, J.C. Bea, K.W. Lee, T. Tanaka, M. Koyanagi, NICHe

The dependence of device reliability on the lattice perfectness of the active silicon in the high-density 3D-LSIs containing through-silicon via (TSV) and micro-bump is extensively investigated using hard X rays at SPring8. The reciprocal lattice space(RLS) data revealed that the Si-lattice structure is largely deteriorated by the thermo-mechanical (TM) stress exerted by Cu-TSVs and CuSn m-bumps, and the local deformation of ultra-thin dies. The TM-stress caused by 20 mm-width Cu-TSV has introduced (i) 3 degrees of the lattice-tilt (mis-orientation) and (ii) 8.3 % decrease in d-space values for Si(004)lattice plane of 3D-LSI chip at 300 ℃. This d-space change has caused a maximum strain up to -0.96% that corresponds to -1300 MPa of compressive stress. The locally deformed upper thinned LSI die having 30 um-thickness is experiencing as high as 4.9 % increase in d-spacing value and the lattice tilt to 0.65 degree after the under-fill cure. More importantly, the lower 300 um-thick active/passive interposer has also experienced the lattice tilt and the change in d-spacing to the magnitude of around 0.2 degree and 0.4 %, respectively. We have found that the retention period for the stacked memory chip degraded with the decrease in the chip thickness. The median retention time for the DRAM-chip with thicknesses below 30 um has been reduced to one-half the retention period for the 100 um-thick DRAM chip. For the first time we explain the DRAM-retention time degradation with the deterioration of Young modulus and distorted Si-lattice structure in the ultra-thin vertically stacked memory chip. We have minimized the TM stress in the active Si to one-third to that of the original value, the polymer is stable up to 400 ℃ with the CTE value of 20 ppm/K.

2:00 p.m.

7.2 Characterization and Reliability of 3D LSI and SiP (Invited), K.W. Lee, M. Murugesan, J. Beal, T. Fukushima, T. Tanaka, M. Koyanagi, Tohoku University

Reliability challenges in 3D LSI associated with mechanical constraints induced by Cu TSVs, μ-bumps and crystal defects, crystallinity in thinned Si wafer and metal contamination induced by Cu diffusion from TSVs and thinned backside surface are mainly discussed. Mechanical stresses induced by Cu TSVs and μ-bumps are strongly dependent on design rules and process parameters. DRAM retention characteristics were severely degraded by Si thinning, especially below 30 μ-m thickness. Minority carrier lifetime was seriously degraded by Cu diffusion from Cu TSVs as the blocking property of barrier layer in TSV is not sufficient. A dry polish (DP) treatment produced a superior extrinsic gettering (EG) layer to Cu diffusion at the backside. We suggest the nondestructive failure analysis using X-ray CT-scan to characterize TSVs connection and μ-bumps joining in 3D stacked LSIs.

2:25 p.m.

7.3 Innovative ESD protections for UTBB FD-SOI Technology, Y. Solaro, P. Fonteneau, C.A. Legrand, D. Marin-Cudraz, J. Passieux, P. Guyader, L.R. Clement, C. Fenouillet-Beranger, P. Ferrari*, S. Cristoloveanu*, STMicroelectronics, *IMEP-LAHC

We present an innovative set of UTBB (Ultra-Thin Body and BOX) ESD protection devices, which achieves remarkable performance in terms of leakage current and triggering control. Ultra-low leakage current below 0.1 pA/μm and adjustable triggering ($1.1V < Vt1 < 2.6V$) capability are demonstrated. These devices rely on gate-controlled injection barriers and match the 28nm UTBB-FDSOI ESD design window by triggering before the nominal breakdown voltage of digital core MOS transistors.

2:50 p.m.

7.4 Comparison of Self-Heating Effect (SHE) in Short-Channel Bulk and Ultra-Thin BOX SOI MOSFETs: Impacts of Doped Well, Ambient Temperature, and SOI/BOX Thicknesses on SHE, T. Takahashi, T. Matsuki*, T. Shinada*, Y. Inoue*, K. Uchida, Keio University, *TIA Headquarters, AIST

Self-heating effects of bulk and SOI FETs including 6-nm ultra-thin (UT) BOX devices are systematically investigated and compared using the four-terminal gate resistance method. For bulk FETs, it is clarified, for the first time, that SHE is not negligible in nanoscale devices mainly due to a decrease in the thermal conductivity of heavily doped well. For SOI FETs, the impacts of the BOX/SOI thinning are evaluated and explained by thermal conductivities of materials in heat dissipation paths. It is demonstrated that the channel temperature of 6-nm UT BOX SOI FETs are close to that of bulk FETs at a chip temperature under operations. A thermal-aware device design of the UT Body and BOX (UTBB) structure is proposed based on evaluated BOX/SOI thickness dependences of SHE. The SHE of UTBB FETs with raised S/D and/or contact pitch scaling could be comparable to that of bulk FETs in deeply scaled nodes.

3:15 p.m.
7.5 Nanowire Variability Impact on Performance and Reliability of Gate-All-Around III-V MOSFETs, S. Shin, M. Masuduzzaman, J. Gu, M. Wahab, N. Conrad, M. Si, P.D. Ye, M. Alam, Purdue University

Three-dimensional electrostatic control of MOSFET channel is essential for technologies beyond the 20nm node. The Gate-all-around (GAA) MOSFET is one such structure that ensures surrounding-gate electrostatic control of each channel/nanowire (NW). An intrinsic trade-off of such a device geometry is the reduced limited channel cross-section area per NW, and thus, several NWs connected in parallel, along with high mobility materials such as InGaAs, are required to achieve the desired drive current, (I_{ON}). Currently, we know of no reports in the literature that explores performance and reliability of GAA MOSFET as a function of the number of NWs (#NW) within a single transistor. In this paper, we (i) examine how the overall performance matrix (e.g., I_{ON}, I_{OFF}, V_{th}, SS, R_C) depends on the number of parallel NWs, (ii) theoretically interpret the results in terms of variability and self- heating among the NWs, (iii) compare the reliability of multiple NW devices (ΔV_{th}, ΔSS, both stress and recovery) with a planar device of similar technology. We find that the self-heating and NW-to-NW variability are reflected in novel properties features of variability and reliability that are neither anticipated nor observed in the corresponding planar technology.

3:40 p.m.
7.6 High Field Transport Characterization in Nano MOSFETs Using 10GHz Sapacitance Measurements, C. Diouf, A. Cros, D. Gloria, J. Rosa, M. Buczko, G. Ghibaudo*, STMICROELECTRONICS, *IMEP-LAHC

With the continuous scaling down, getting information about electronic transport in MOSFETs operating at high drain voltage is a challenging topic. The carrier mobility is usually extracted in the linear regime but becomes irrelevant in the saturation region, where non-stationnary transport phenomena become of paramount importance [1]. In addition, velocity is not reliably extracted at high drain voltage because of uncertainty in the inversion charge evaluation. In this paper, 10 GHz capacitance measurements are performed, for the first time, in ultra-scaled MOS devices in order to consistently extract the inversion charge and average velocity up to saturation regime. Obtained saturation and linear ballistic rate allow to evidence and quantify non-negligible non-stationnary transport phenomenon in very short devices.

Session 8 – FOCUS SESSION: Sensors, MEMS, and BioMEMS – Sensors and Microsystems for Biomedical Applications
Monday, December 9, 1:30 p.m.
Columbia Rooms 5&7

Co-Chairs: *Youri Ponomerov, NXP Semiconductor*
Tian-Ling Ren, Tsinghua University

1:35 p.m.
8.1 Development of the Ion Torrent CMOS Chip for DNA Sequencing (Invited), J. Bustillo, K. Fife, B. Merriman, J. Rothberg, Life Technologies Inc.

Since the landmark discovery of Watson and Crick in 1953 that biological information was encoded in DNA as a sequence of chemical building-block "letters", developing technology for reading—or "sequencing"—this chemical code has been the most fundamental problem in all of biosensing. Techniques that first enabled this were invented by Sanger in 1978, and were taken to massively parallel form by Rothberg in 2005 [1], which in turn ushered in the current era of genome sequencing for biomedical research. As with many other important applications in sensing and information processing—such imaging—there is a critical, transformative disruption that comes from transferring it onto a CMOS chip, due to the economic power of the CMOS industry to advance mass manufacturing capabilities in accordance with Moore's Law. Thus, devising a way to perform high-throughput DNA Sequencing on a CMOS chip could be expected to similarly transform the use of DNA sequencing. In particular, this will enable the emerging field of personalized medicine based on individual genome sequence, which requires deploying low cost, high quality, mass manufactured sequencing devices at a global population scale.

2:00 p.m.
8.2 3D Biomimetic Hair Sensors and Actuators (Invited), K. Najafi, University of Michigan

This paper will provide an overview of biomimetic hair-like sensors and actuators. A new class of biomimetic devices has been developed. Advantages and features of these devices will be presented.

2:25 p.m.
8.3 Digital Approaches in Electronic Biochips (Invited), C. Guiducci, E. Accastelli, F. Spiga, EPFL

In what follows, we will analyze the peculiar advantages of electronic biochips together with their critical limitations and we will discuss how new technological (ultra-miniaturized devices) and system design approaches for bioanalytical miniaturized systems can overcome the present issues and lead to unforeseen possibilities in the life science domain.

2:50 p.m.
8.4 CMOS Biosensor Devices and Applications (Invited), M. Reed, Yale

The detection of extremely low concentrations of small molecules, including proteins, DNA, and biomarkers, has tremendous applications for translational medicine and fundamental studies. This talk will discuss the emerging field of integrated silicon nanowire bioFETs for the direct, label-free detection of biomolecules with unprecedented sensitivity and scalability.

3:15 p.m.
8.5 Ultraflexible Organic Devices for Biomedical Applications (Invited), T. Someya, T. Sekitani, M. Kaltenbrunner, T. Yokota, H. Fuketa*, M. Takamiya*, T. Sakurai*, University of Tokyo, *Japan Science and Technology Agency (JST)

We have successfully manufactured ultrathin and ultra-lightweight soft organic thin-film transistors and integrated circuits including a two-dimensional array of amplifiers on polymeric films with a thickness of

only 1.2 μm. The transistor films exhibit extraordinarily tough mechanical robustness such as minimum bending radius of 5 μm.

3:40 p.m.
8.6 Implantable Neural Probes for Chronic Electrical Recording and Optical Stimulation (Invited), F. Wu, E. Stark*, G. Buzsaki*, L. Tien**, D. Kaplan**, F. Chen, J. Berke, K. Wise, E. Yoon, University of Michigan, *New York University, **Tufts University

We review and report the recent progress in neural probe technologies for chronic electrical recording and optical stimulation. We introduce the silicon optical probes monolithically integrated with optical waveguide and the flexible polymer probes for reducing micromotion-induced tissue damage, followed by in-vivo measurement results to validate the corresponding technical approaches.

4:05 p.m.
8.7 Labs-on-a-Chip and Nanosensors for Medical Applications and life Sciences (Invited), A. van den Berg, University of Twente

The recent rapid developments in microfluidics technologies has enabled the realization of miniaturized laboratories. These Labs-on-a-Chip will play an important role in future medicine, both in point-of-care devices for drug or biomarker monitoring, as well as in early diagnostic devices. We developed a pre-filled ready-to-use capillary electrophoresis platform for measuring ions in blood. It is used to monitor lithium in finger-prick blood of manic-depressive patients, but can also be used for measuring calcium in blood for prevention of milk fever, or for measuring creatinine in blood or sodium in urine for early detection of ESRD. Another device was developed for analyzing male fertility by determining sperm concentration and motility in semen. It appears that the same device can be easily adapted to detect the presence of cells in milk, a good indicator for the presence of mastitis.For early detection of colon cancer, nanowire sensors for detection of hypermethylated DNA will be presented, showing label-free DNA detection. The small size of these nanowire sensors enables the integration of a complete lab in a pill, that may be used as a screening tool for early diagnostics of intestinal cancer. Finally, nanogap structures for sensitive SERS detection will be presented.

Session 9: Circuit and Device Interaction – Advanced CMOS Technology Platform
Tuesday, December 10, 9:00 a.m.
International Ballroom Center
Co-Chairs: Ali Keshavarzi, Cypress Semiconductor
Shyh-Horng Yang, TSMC

9:05 a.m.
9.1 A 16nm FinFET CMOS Technology for Mobile SoC and Computing Applications, S.-Y. Wu, C.Y. Lin, M.C. Chiang, J.J. Liaw, J.Y. Cheng, S.H. Yang, M. Liang, T. Miyashita, C.H. Tsai, B.C. Hsu, S.Y. Chang, V.S. Chang, C.H. Chang, J.H. Chen, H.F. Chen, K.C. Ting, Y.K. Wu, K.H. Pan, R.F. Tsui, C.H. Yao, T.L. Lee, P.R. Chang, H.M. Lien, W. Chang, H.M. Lee, C.C. Chen, T. Chang, R. Chen, M. Yeh, Y.H. Chiu, M.H. Tsai, S.M. Jang, K.S. Chen, Y. Ku, Tawiwan Semiconducor Manufacturing Company

For the first time, we present a state-of-the-art energy-efficient 16nm technology integrated with FinFET transistors, 0.07um^2 high density (HD) SRAM, Cu/low-k interconnect and high density MiM for mobile SoC and computing applications. This technology provides 2X logic density and >35% speed gain or >55% power reduction over our 28nm HK/MG planar technology. To our knowledge, this is the smallest fully functional 128Mb HD FinFET SRAM (with single fin) test-chip demonstrated with low Vccmin for

16nm node. Low leakage (SVt) FinFET transistors achieve excellent short channel control with DIBL of <30 mV/V and superior Idsat of 520/525 uA/um at 0.75V and Ioff of 30 pA/um for NMOS and PMOS, respectively.

9:30 a.m.
9.2 High Performance UTBB FDSOI Devices Featuring 20nm Gate Length for 14nm Node and Beyond, Q. Liu, M. Vinet*, J. Gimbert, N. Loubet, R. Wacquez*, L. Grenouillet*, Y.L. Tiec*, A. Khakifirooz**, T. Nagumo***, K. Cheng**, H. Kothari, D. Chanemougame, F. Chafik, S. Guillaumet, J. Kuss**, F. Allibert^, G. Tsutsui**, J. Li**, P. Morin, S. Mehta**, R. Johnson**, L.F. Edge**, S. Ponoth**, T. Levin**, S. Kanakasabapathy**, B. Haran**, H. Bu**, J.-L. Bataillon, O. Weber*, O. Faynot*, E. Josse, M. Haond, W. Kleemeier, M. Khare**, T. Skotnicki, S. Luning^^, B. Doris**, M. Celik, R. Sampson, STMicroelectronics, *CEA-LETI, **IBM, ***Renesas, ^SOITEC, ^^GLOBALFOUNDRIES

We report high performance UTBB FDSOI devices with LG at 20nm. Competitive drive current (1120/1220 μA/μm for N/PFET at 100nA/μm off current) and excellent electrostatics are achieved. Low cSiGe PFET AVt is presented for the first time. It is also demonstrated that FDSOI reliability is superior to Bulk devices.

9:55 a.m.
9.3 Monolithic 3D Chip Integrated with 500ns NVM, 3ps Logic Circuits and SRAM, C.-H. Shen, J.-M. Shieh, W.-H. Huang, T.-T. Wu, B.-Y. Chen, G.-W. Huang, Y.-C. Lien*, C.-F. Chen**, M.-F. Chang**, C. Hu***, F.-L. Yang, National Nano Device Laboratories, *Stanford University, **National Tsing Hua University, ***University of California, Berkeley

For the first time, a sequentially processed sub-50nm monolithic 3D IC with integrated logic/NVM circuits and SRAM is demonstrated using multiple layers of ultrathin-body (UTB) MOSFET-based circuits interconnected through 300nm-thick interlayer dielectric (ILD). High-performance sub-50nm UTB MOSFETs using deposited ultra-flat and ultra-thin (20nm) epi-like Si enable across-layer and in-layer high-speed 3ps logic circuits and 1-T 500ns plasma-MONOS NVMs as well as 6T SRAMs with static noise margin of 280 mV and reduced footprint by 25%. Closely stacked monolithic 3D circuits envision advanced high-performance, rich function, and low power intelligent mobile devices.

10:20 a.m.
9.4 2nd Generation Dual-Channel Optimization with cSiGe for 22nm HP Technology and Beyond, C. Ortolland, D. Jaeger, T. Mcardle, C. Dewan, R. Robison, K. Zhao, J. Cai, P. Chang, Y. Liu, D. Ioannou, P. Oldiges, P. Agnello, S. Narasimha, V. Narayanan, G. Freeman, IBM

In this paper we report on a comprehensive study of Silicon-Germanium channel (cSiGe) physics, layout effects and impact on device performance. This work demonstrates a 2nd generation of dual channel technology, which meets the 22nm high performance (HP) requirement. Modeling and simulation are used to optimize the process to obtain 20% performance boost and 10% Short Channel Effect (SCE) improvement. This 2nd generation high performance dual channel process has been integrated into a manufacturable and yieldable technology, thereby providing a solid platform for introduction of SiGe FinFet technology

10:45 a.m.
9.5 Retention Time Optimization for eDRAM in 22nm Tri-Gate CMOS Technology, Y. Wang, N. Bisnik, R. Brain, F. Hamzaoglu, N. Lindert, M. Meterelliyoz, J. Park, S. Tomishima, A. Umut, K. Zhang, Intel Corporation

A high performance eDRAM technology has been developed based on a high-performance and low-power 22nm tri-gate CMOS process. By applying noise reduction techniques and extensive device and design co-optimization, over 100µs retention time at 95°C has been achieved for a Gbit array with robust manufacturing yield.

11:10 a.m.
9.6 Embedded FLOTOX Flash on Ultra-Low Power 55nm Logic DDC Platform, M. Hori, K. Fujita, M. Yasuda, K. Ookoshi, M. Tsutsumi, H. Ogawa, M. Takahashi, T. Ema, Fujitsu Semiconductor Ltd.

We have successfully embedded flash on an ultra-low power 55nm DDC platform. In spite of reduced thermal budget of DDC process, single-bit charge loss of flash after cycling is comparable to that of baseline embedded flash. Improved variability and resultant ultra-low power digital performance of the DDC process is maintained.

11:35 a.m.
9.7 Innovations in Special Constructs for Standard Cell Libraries in Sub 28nm Technologies (Invited), M. Rashed, M. Tarabbia, J. Kim, N. Jain, S. Ahmed, I. Rahim, J. Kim, I. Lin, S. Chan, H. Yoshida, S. Beasor, L. Yuan, J. Kye, J. Chee, S. Johnson, U. Schroeder, N. Cave, T. Tang, S. Kengeri, S. Venkatesan, GLOBALFOUNDRIES

The breakthrough in middle of line local interconnect is realized by the innovative "Special construct based approach" first proposed in the ISDA alliance by GLOBALFOUNDRIES where SRAM like local interconnect "connectivity shapes" were carefully constructed and validated by respective Litho and process integration models in the context of random logic. These constructs were then validated in Silicon by carefully chosen design of experiments in Technology Qualification and Validation Testchips as well as SOC based Design Testchips. In this paper, we will explain and provide some critical illustrations how these special constructs have enabled the GLOBALFOUNDRIES 20nm technology to offer Industry's most compelling technology solutions for power, performance and cost metrics that cover the entire range of semiconductor product landscape. These innovations in "Special Constructs" based MOL local interconnects along with optimum M1 Litho solution and 80nm 1.3x metal adoption led the way to achieve industry's most optimum 20nm technology offerings. These constructs are also fully re-used in our 14nm FinFET Technology with significant PPA advantages without having to scale Poly or Metal Pitch.

Session 10: Memory Technology – RRAM and FERAM
Tuesday, December 10, 9:00 a.m.
International Ballroom East
Co-Chairs: Sabina Spiga, CNR-IMM, Laboratorio MDM
Chrong Jung Lin, National Tsing-Hua University

9:05 a.m.
10.1 Improvement of Data Retention in HfO_2 / Hf 1T1R RRAM Cell Under Low Operating Current, Y. Chen, M. Komura*, R. Degraeve, B. Govoreanu, L. Goux, A. Fantini, N. Raghavan, S. Clima, L. Zhang, A. Belmonte, A. Redolfi, G.S. Kar, G. Groeseneken, D. Wouters, M. Jurczak, imec, *Toshiba assignee at imec

In this study, we identify the mobile oxygen diffusion from oxygen scavenging layer as a dominant controlling parameter in determining the retention degradation in HfO_2 based RRAM. By limiting the oxygen diffusion with an additional annealing applied after RRAM cell formation, the retention has been

greatly improved. Electrical tuning of drifting the mobile oxygen further away also improves the retention without increasing the switching current.

9:30 a.m.
10.2 Vacancy-Modulated Conductive Oxide Resistive RAM (VMCO-RRAM): An Area-Scalable Switching Current, Self-Compliant, Highly-Nonlinear and Wide On/Off-Window Resistive Switching Cell, B. Govoreanu, A. Redolfi, L. Zhang, C. Adelmann, M. Popovici, S. Clima, H. Hody, V. Paraschiv, I. Radu, A. Franquet, J.-C. Liu, J. Swerts, O. Richard, H. Bender, L. Altimime, M. Jurczak, imec

In this work, we report a novel self-compliant and self-rectifying resistive switching memory cell, with area-scalable switching currents, featuring a set current density of ~5nA/nm^2 (<9uA for a 40nm-size cell), high program nonlinearity exceeding 100 and low reset current density of <0.6nA/nm^2 (<1uA@40nm size). The cell can be operated at below ±4V/10ns, with a large on/off window of >100 and retention extrapolates to 10yr at 101˚C. The switching stack is fully based on ALD processes, using common high-k dielectrics and has a thickness of <10nm, meeting 3D Vertical RRAM requirements. Moreover, we point out the nonlinearity–low-current operation interdependence and discuss the scaling potential of areal switching RRAM for reliable sub-uA current operation in the 10nm-cell size realm.

9:55 a.m.
10.3 Ultra High Density 3D Via RRAM in Pure 28nm CMOS Process, M.C. Hsieh, Y.C. Liao, Y.W. Chin, T.S. Chang*, Y.D. Chih*, M.J. Tsai**, Y.C. King, C.J. Lin, National Tsing-Hua University, *Taiwan Semiconductor Manufacturing Company, **Industrial Technology Research Institute

In this paper, we present an ultra high density 3D Via RRAM with 28nm HKMG CMOS fully compatible process. It is the first time to report a cross-point 3D RRAM formed by the stacked 30nm Cu Via and Cu metal line of 28nm HKMG CMOS Cu single damascene process. The 3D Via RRAM cell consists of a TaON-based resistive film, Cu Via as top electrode, and Cu metal as bottom electrode. The TaON-based RRAM film is a composite layer of backend metal glue layer of Ta and TaN in 28nm Cu damascene process. Moreover, in the compact 3D Via RRAM structure, the unit area of a single stacked cell-string is reduced to only 4 times of Via size by 28nm CMOS design rules. Since the cross-point 3D Via RRAM is fabricated without extra TMO film or process step, this excellent cell scalability and compatibility can provide a competitive low cost and high density embedded NVM solution in advanced CMOS logic nodes.

10:20 a.m.
10.4 3D Vertical TaO_x/TiO_2 RRAM with over 10^3 Self-Rectifying Ratio and Sub-uA Operating Current, C.W. Hsu, C.C. Wan, I-T. Wang, M.C. Chen, C.L. Lo, Y.J. Lee*, W.Y. Jang**, C.H. Lin**, T.H. Hou, National Chiao Tung University, *National Nano Device Laboratories, *Winbond Electronics Corporation

The 3D double-layer vertical RRAM with ultralow sub-uA operating current and high self-rectifying ratio over 10^3 has been demonstrated for the first time. This $Ta/TaO_x/TiO_2/Ti$ interfacial switching device overcomes the intrinsic trade-off between operating current and variability in filamentary RRAMs and shows promising potential for high-density data storage.

10:45 a.m.
10.5 Nanoscale (~10nm) 3D Vertical ReRAM and NbO_2 Threshold Selector with TiN Electrode, E. Cha, J. Woo, D. Lee, S. Lee, J. Song, Y. Koo, J. Lee, C. Park, M. Yang*, K. Kamiya*, K. Shiraishi*, B. Magyari-Köpe**, Y. Nishi**, H. Hwang, POSTECH, *University of Tsukuba, **Stanford University

We investigated the scaling and 3-D integration issue of NbO_2 threshold selector. To reduce the threshold current for I-M-T, heat confinement is effectively achieved by nanoscale TiN electorde. 1S1R and hybrid devices show excellent resistive switching charactristics with supressing current through sneak-path. 1S1R and hybrid devices exhibit excellent promise for future high density 3-D vertical memory application.

11:10 a.m.
10.6 Selector-less ReRAM with an Excellent Non-Linearity and Reliability by the Band-Gap Engineered Multi-Layer Titanium Oxide and Triangular Shaped AC Pulse, S. Lee, D. Lee, J. Woo, E. Cha, J. Song, J. Park, H. Hwang, POSTECH

The selector-less ReRAM was demonstrated with tunnel barrier modulation by the band-gap engineering of multi-layer TiO_y/TiO_x. It exhibited high non-linearity (~23), excellent AC endurance (~108 cycle), and switching uniformity. It shows a promise for future high density cross-point memory application.

11:35 a.m.
10.7 BEOL Compatible (300°C) $TiN/TiO_x/Ta/TiN$ 3D nanoscale (~10nm) IMT Selector, D. Lee, J. Park, S. Park, J. Woo, K. Moon, E. Cha, S. Lee, J. Song, Y. Koo, H. Hwang, Pohang University of Science and Technology

TiO_x based IMT characteristics were achieved by optimizing oxygen profile and local filament formation. In 3D structure, TiN BE and cell scaling lead to lower I_{off}, Ith, and P_{IMT}, which are directly related with heat confinement effect. TiO_x based IMT selector devices with very low threshold current (sub-uA) fabricated at low process temperature (300°C) show promise for future BEOL ReRAM applications.

12:00 p.m.
10.8 Ferroelectric Hafnium Oxide: A CMOS-Compatible and Highly Scalable Approach to Future Ferroelectric Memories (Invited), J. Müller, T.S. Böscke^, S. Müller*, E. Yurchuk, P. Polakowski, J. Paul, U. Schröder*, A. Kersch***, D. Martin*, S.V. Kalinin^^, S. Riedel, T. Schlösser**, R. Boschke**, R. van Bentum**, T. Mikolajick*, Fraunhofer Center Nanoelectronic Technologies, *NaMLab gGMBH, **GLOBALFOUNDRIES, ***FH-München, ^Bosch Solar Energy, ^^ORNL

Bound to complex perovskite systems, FRAM suffers from limited CMOS-compatibility and faces severe scaling issues in today´s and future technology nodes. The ability to engineer ferroelectricity in HfO_2, a high-k dielectric well established in memory and logic devices, reveals a new perspective for manufacturability and scalability of future 1T and 1T/1C ferroelectric memories.

Session 11: Display and Imaging Systems – Flexible Electronics
Tuesday, December 10, 9:00 a.m.
Georgetown Room
Co-Chairs: *Wolfgang Benecke, Fraunhofer ISIT*
David Gundlach, NIST

9:05 a.m.
11.1 A Flexible Ultra-Thin-Body SOI Single-Photon Avalanche Diode, P. Sun, B. Mimoun, E. Charbon, R. Ishihara, Delft University of Technology

The world's first flexible ultra-thin-body SOI single-photon avalanche diode (SPAD) is reported by device layer transfer to plastic with peak PDP at 11%, DCR around 20kHz and negligible afterpulsing and cross-talk. It compares favorably with CMOS SPADs while it can operate both in FSI and BSI with 10mm bend diameter.

9:30 a.m.

11.2 Film Profile Engineering (FPE): A New Concept for Manufacturing of Short-Channel Metal Oxide TFTs, R.-J. Lyu, H.-C. Lin, M.-H. Wu, B.-S. Shie, H.-T. Hung, T.-Y. Huang, National Chiao Tung University

A film profile engineering (FPE) concept which utilizes the unique features of various deposition tools to tailor and optimize the profile of the deposited films was demonstrated with the fabricated ZnO TFTs. By implementing the PR trimming technique, high performance devices with L < 100 nm can be readily achieved.

9:55 a.m.

11.3 Integrated UHF a-IGZO Energy Harvester for Passive RFID Tags, A. Chasin, V. Volskiy*, M. Libois, M. Ameys, M. Nag, M. Rockele, K. Myny, S. Steudel, S. Schols, G. Vandenbosch*, W. de Raedt, J. Genoe, G. Gielen*, P. Heremans, imec, *KU Leuven

Thin-film circuits fabricated directly on plastic foil are contenders for low-cost RFID tags. Preferably, such tags are passive, i.e. powered by the electromagnetic wave sent by the receiver. To that end, a rectifier is required on the tag. Here, we show for the first time a fully integrated energy harvester based on low temperature processed amorphous IGZO (Indium-Gallium-Zinc Oxide) semiconductor operating at 868MHz. The harvester supplies more than 1Vdc to a resistive load at a distance of 15cm from the power emitter.

10:20 a.m.

11.4 Mechanically Flexible Vertically Integrated a-IGZO Thin-Film Transistors with 500 nm Channel Length Fabricated on Free Standing Plastic Foil, L. Petti, P. Aguirre, N. Münzenrieder, G. A. Salvatore, C. Zysset, A. Frutiger, L. Büthe, C. Vogt, G. Tröster, Electronics Laboratory, Swiss Federal Institute of Technology

First flexible InGaZnO vertical-TFTs (VTFTs) with 500 nm channel, fabricated on free-standing plastic foil, are reported. VTFTs show on/off ratio of 10^7 and threshold voltage of 2.2 V. Functionality to 5 mm bending radius, after 1000 bending cycles is demonstrated. VTFTs are proven to be suitable for compact bendable electronics.

10:45 a.m.

11.5 High Electron Mobility (>16 cm^2/Vsec) FETs with High On/Off Ratio (>10^6) and Highly Conductive Films (σ>10^2 S/cm) by Chemical Doping in Very Thin (~20 nm) TiO_2 Films on Thermally Grown SiO_2, G. Oike, T. Yajima, T. Nishimura, K. Nagashio, A. Toriumi, The University of Tokyo

We have investigated the electrical conduction of TiO_2 films by both field-effect and chemical doping. We report that FET characteristics of TiO_2 are much improved (>16 cm^2/Vsec and on/off ratio >10^5, and that its conductivity is also significantly increased up to 10^2 S/cm by chemical doping. The results are quite promising for both TFT and transparent electrode applications of TiO_2.

11:10 a.m.

11.6 Inkjet Printed Polymer SRAM-cell Design for Flexible FPGA with Physical Parameter-Based TFT Model, J. Jang, J. Lee, H. Kim, J. Lee*, J.W. Chung*, B. Lee*, D.M. Kim, S.-J. Choi, D.H. Kim, Kookmin University, *Samsung Advanced Institute of Technology

We developed a circuit simulator for polymer-based circuits and systems. The analytical model was established from experimentally extracted parameters. The model was incorporated into HSPICE, and verified by the simulation result compared with the measured data error within 3%. Furthermore, we designed SRAM-cell circuits using the proposed circuit simulator.

11:35 a.m.
11.7 Local Transfer of Single-Crystalline Silicon (100) Layer by Meniscus Force and Its Application to High-Performance MOSFET Fabrication on Glass Substrate, M. Akazawa, K. Sakaike, S. Nakamura, T. Fukunaga, S. Hayashi, S. Morisaki, S. Higashi, Hiroshima University

We propose a novel low-temperature local layer transfer technique using meniscus force. Local transfer of the thermally-oxidized SOI layer to glass was carried out without any problem. The n-channel MOSFET fabricated on glass using the SOI layer showed very high mobility of 742 $cm^2V^{-1}s^{-1}$, low threshold voltage of 1.5 V.

Session 12: Modeling and Simulation – Technology CAD (TCAD)
Tuesday, December 10, 9:00 a.m.
Jefferson Room
Co-Chairs: Jeff Wu, TSMC
Zhiping Yu, Tsinghua University

9:05 a.m.
12.1 The Impact of Increased Deformation Potential at MOS Interface on Quasi-Ballistic Transport in Ultrathin Channel MOSFETs Scaled down to Sub-10 nm Channel Length, S. Koba, R. Ishida, Y. Kubota, H. Tsuchiya, Y. Kamakura*, N. Mori*, M. Ogawa, Kobe University, *Osaka University

Against a common view that ballistic transport is enhanced due to channel length scaling, it is demonstrated for the first time that ballistic transport is not necessarily enhanced in ultra-scaled MOSFETs due to intensified acoustic phonon scattering, based on Monte Carlo simulation considering an increased deformation potential at MOS interfaces.

9:30 a.m.
12.2 Physical Understanding of Alloy Scattering in SiGe Channel for High-Performance Strained pFETs, C. Jeong, H.-H. Park*, S. Dhar, S. Park, K. Lee, S. Jin*, W Choi*, U.-H. Kwon, K.-H. Lee, Y. Park, Samsung Electronics Co. Ltd., *Samsung Semiconductor Inc.

For devices beyond the 14nm node, it is important to investigate performance boosters such as high mobility channels. Although pure Ge offers a higher hole mobility than Si, conventional problems like surface passivation and its integration with Si makes SiGe alloy with low Ge mole fraction a viable option. The significance of alloy scattering, however, has been widely debated [1-3], so the accurate modeling of alloy scattering in SiGe channel has become an important issue to predict the performance of future SiGe-based FETs. Usually, the calculation of alloy scattering mobility assumes an alloy scattering center in a simple analytical form with some fitting parameters, which is a good practical approach but has a limited predictability. In this paper, an atomistic tight-binding simulation is used to study alloy scattering in SiGe-based FETs, and to compare with experimental data. We conclude (i) although it is essentially impossible to avoid alloy scattering in SiGe material, (ii) high-mobility is indeed achieved in SiGe channel by combining lattice-mismatch stresses from Si virtual substrate with stresses from Source/Drain(SD) stressor.

9:55 a.m.
12.3 Quantum-Barriers and Ground-Plane Isolation: A Path for Scaling Bulk-FinFET Technologies to the 7 nm-node and Beyond, G. Eneman, G. Hellings, A. De Keersgieter, N. Collaert, A. Thean, imec

The electrostatic integrity of 7 nm-node bulk FinFETs (FF) is studied by TCAD. Lowly-doped bulk-FF have worse electrostatics than SOI-FF or gate-all-around (GAA) FETs. However, by introducing a 200 meV band offset/quantum barrier (QB) under the channel or a > 1e18 doped ground-plane (GP), the electrostatics of bulk-FF match those of SOI-FF and GAA for the 7 nm-node. For sufficient substrate isolation, the band offset must be positioned within 5 nm of the STI edge. The QB layer that provides the offset can be thinned down to 10 nm. A GP is more robust to variations in position, but thinning this layer requires doping levels that are undesired especially for Ge. Bulk-FF with GP or QB isolation show good scalability to the 5 nm-node, improving both IEFF and DIBL.

10:20 a.m.
12.4 UTSOI2: A Complete Physical Compact Model for UTBB and Independent Double Gate MOSFETs, T. Poiroux, O. Rozeau, S. Martinie, P. Scheer*, S. Puget*, M.A. Jaud, S. El Ghouli*, J.C. Barbé, A. Juge*, O. Faynot, CEA-LETI, *STMicroelectronics

We present a complete physical compact model dedicated to Ultra-Thin Body and Box technology and able to describe accurately independent double gate operation. Its physical background makes it predictive and all included effects make it suitable for sub-20nm nodes. It meets standard Quality and Robustness tests for circuit design applications.

10:45 a.m.
12.5 Mobility in High-K Metal Gate UTBB-FDSOI Devices: From NEGF to TCAD Perspectives (Invited), D. Rideau, Y. Niquet, O. Nier, A. Cros, P. Palestri***, D. Esseni, V.H. Nguyen*, F. Triozon**, J.C. Barbé**, I. Duchemin*, D. Garetto^, L. Smith^, L. Silvestri^, F. Nallet^, R. Clerc^^, J.P. Manceau^^^, O. Weber**, F. Andrieu**, E. Josse, C. Tavernier, H. Jaouen, STMicroelectronics, *SP2M, UMR-E CEA/UJF, **CEA-LETI, ***DIEGM, University of Udine, ^Synopsys, ^^Laboratoire Hubert Curien & Institut d'Optique, ^^^IBM

This paper aims to review important theoretical and experimental aspects of both electrostatics and channel mobility in High-K Metal Gate UTBB-FDSOI MOSFETs. A simulation chain, including advanced quantum solvers, and semi-empirical Technology Computer Assisted Design (TCAD) tools is presented.

11:10 a.m.
12.6 Exploring the Design Space of Non-Planar Channels: Shape, Orientation, and Strain, Z. Stanojevic, M. Karner*, H. Kosina, Institute for Microelectronics, TU Wien, *Global TCAD Solutions GmbH

We present a consistent simulation framework for rapid evaluation of non-planar device designs. Modeling is physics-based and combines a self-consistent Schrodinger-Poisson solver, k*p band structure description, and linearized Boltzmann transport. In contrast to common TCAD tools, our framework is virtually free of fit-parameters and inherently captures carrier confinement, channel and interface orientation, surface roughness scattering, and arbitrary strain.

11:35 a.m.
12.7 Threshold Behavior of the Drift Region: the Missing Piece in LDMOS Modeling, S. Sque, A. Scholten, A. Aarts, D. Klaassen, NXP Semiconductors

Most LDMOS compact models fail to accurately reproduce the internal-drain potential and on-state capacitances, which are shown to be related. TCAD simulations show that the drift region exhibits threshold-like behavior. A two-transistor model can accurately model the internal-drain potential and hence (simulated and measured) capacitances.

12:00 p.m.
12.8 Copper Through Silicon Via Induced Keep Out Zone for 10nm Node Bulk FinFET CMOS Technology, W. Guo, V. Moroz*, G. Van der Plas, M. Choi*, A. Redolfi, L. Smith*, G. Eneman, S. Van Huylenbroeck, P.D. Su, A. Ivankovic, B. De Wachter, I. Debusschere, K. Croes, I. De Wolf, A. Mercha, G. Beyer, B. Swinnen, E. Beyne, IMEC, *Synopsys, Inc.

This work provides for the first time comprehensive and early guidelines for TSV integration in 10nm node FinFET technology. The key contributors to the TSV induced Keep Out Zone for FinFETs are analyzed. Advanced TCAD sub-band modeling of the stress impact on mobility is verified by uniaxial wafer bending experiments.

Session 13 – FOCUS SESSION: Process and Manufacturing Technology – Advanced Processing and Platforms for Manufacuring and More than Moore Applications
Tuesday, December 10, 9:00 a.m.
Lincoln Room
Co-Chairs: Sangjin Hyun, Samsung
Jeff Hull, Micron

9:05 a.m.
13.1 Challenges in 3D Memory Manufacturing and Process Integration (Invited), N. Chandrasekaran, Micron Technology

Memory industry transition from planar to 3D scaling and introduction of several emerging memory devices into manufacturing over the next decade is going to drive several new and unique challenges. The inflection point we are faced with is a new paradigm where advancements in materials science, equipment technology, and control methodologies are critical for scaling cadence. This paper discusses these challenges and inflection point faced by the Semiconductor memory industry.

9:30 a.m.
13.2 LED Manufacturing Issues Concerning Gallium Nitride-on-Silicon (GaN-on-Si) Technology and Wafer Scale up Challenges (Invited), S. Nunoue, T. Hikosaka, H. Yoshida, J. Tajima, S. Kimura, N. Sugiyama, K. Tachibana, T. Shioda, T. Sato, E. Muramoto, M. Onomura, Toshiba Corporation

The light output power at high temperature required for LED applied in solid-state lighting can be obtained by reducing TDD on Si substrate using a new technology in which SiN multiple-modulation interlayer is used. We have realized highly efficient blue LEDs were grown on high-crystalline-quality GaN templates on 8-inch Si.

9:55 a.m.
13.3 A Multi-Wavelength 3D-Compatible Silicon Photonics Platform on 300mm SOI Wafers for 25Gb/s Applications, F. Boeuf, S. Crémer, N. Vulliet, T. Pinguet*, A. Mekis*, G. Masini*, L. Verslegers*, P. Sun*, A. Ayazi*, N-K. Hon*, S. Sahni*, Y. Chi*, B. Orlando, D. Ristoiu, A. Farcy, F. Leverd, L. Broussous, D. Pelissier-Tanon, C. Richard, L. Pinzelli, R. Beneyton, O. Gourhant, E. Gourvest, Y. Le-Friec, D. Monnier, P. Brun, M. Guillermet, D. Benoit, K. Haxaire, J.R. Manouvirer, S.

Jan, H. Petiton, J.F. Carpentier, T. Quémerais, C. Durand, D. Gloria, M. Fourel, E. Batail, F. Baron, P. Delpech, L. Salager, P. De Dobbelaere*, B. Sautreuil, STMicroelectronics, *Luxtera

Recently Silicon Photonics has generated an outstanding interest for integrated optical communications. In this paper we describe a 300mm Silicon Photonics platform designed for 25Gb/s and above applications at the three typical communication wavelengths and compatible with 3D integration. Main process features and device results are described.

10:20 a.m.
13.4 300mm Size Ultra-Thin Glass Interposer Technology and High-Q Embedded Helical Inductor (EHI) for Mobile Application, W.-C. Lai, H.-H. Chuang, C.-H. Tsai, E.-H. Yeh, C.-H. Lin, T.-H. Peng, L.-J. Yen, W.-S. Liao, J.-N. Hung, C.-C. Sheu, C.-H. Yu, C.-T. Wang, K.-C. Yee, D. Yu, Taiwan Semiconductor Manufacturing Company

The first publication on fabrication of a 300 mm size, 50 μm ultra-thin glass interposer is presented. Merits of on-glass inductors and transmission lines outperform those of on-silicon in Q-factor, power dissipation, and power/signal integrity. Glass interposer is a promising solution for future high frequency mobile RF application.

10:45 a.m.
13.5 Comprehensive Study of Effective Current Variability and MOSFET Parameter Correlations in 14nm Multi-Fin SOI FINFETs, A. Paul, A. Bryant, T. Hook*, C.C. Yeh, V. Kamineni, J.B. Johnson*, N. Tripathi, T. Yamashita, G. Tsutsui, V. Basker, T.E. Standaert, J. Faltermeier, B.S. Haran, S. Kanakasabapathy, H. Bu, J. Cho, J. Iacoponi, M. Khare, GLOBALFOUNDRIES Inc., *IBM Microelectronics

A first time rigorous experimental study of effective current (I_{eff}) variability in high-volume manufacturable (HVM) 14nm Silicon-On-Insulator (SOI) FINFETs is reported which identifies, threshold voltage (Vtlin), external resistance (Rext), and channel trans-conductance (Gm) as three independent sources of variation. The variability in Gm, Vtlin (A_{VT}=1.4(n)/0.7(p) mV-μm), and Ieff exhibit a linear Pelgrom fit indicating local variations, along with non-zero intercept which suggests the presence of global variations at the wafer level. Relative contribution of Gm to Ieff variability is dominant in FINFETs with small number of fins (Nfin); however, both Gm and Rext variations dominate in large Nfin devices. Relative contribution of Vtlin remains almost independent of Nfin. Both n and p FINFETs show the above mentioned trends.

11:10 a.m.
13.6 Opportunities and Challenges of the 450mm Transition (Invited), J. Lin, P. Lin, Taiwan Semiconductor Manufacturing Company

The 450mm transition is a great opportunity to reduce the die cost and stimulate another wave of innovations and greener manufacturing. There are many challenges ahead including tool productivity, uniformity, precision, cost-of-ownership reduction, and green concept design-in tool and manufacturing systems. These key challenges will be discussed in this paper.

Session 14: Sensors, MEMS, and BioMEMS – BioMEMS and BioSensors
Tuesday, December 10, 9:00 a.m.
Columbia Rooms 5&7
Co-Chairs: Yuji Miyahara, Tokyo Medical and Dental University
Pamela Bhatti, Georgia Institute of Technology

9:05 a.m.
14.1 200 mm Wafer-Scale Integration of Sub-20 nm Sacrificial Nanofluidic Channels for Manipulating and Imaging Single DNA Molecules, C. Wang, S.-W. Nam, J. Cotte, H. Peng, C. Jahnes, D. Wang, R. Bruce, M. Guillorn, L. Gignac, W. Advocate, C. Breslin, M. Brink, J. Bucchignano, E. Duch, A. Galan, E. Kratschmer, P.J. Litwinowicz, M. Lofaro, W. Price, S.M. Rossnagel, R.D. Goldblatt, E.A. Joseph, D. Pfeiffer, S. Pap Rao, A. Royyuru, G. Stolovitzky, E. Colgan, Q. Lin, S. Polonsky, IBM T.J. Watson Research Center

We report sub-20 nm sacrificial nanochannels that enable stretching and translocating single DNA molecules. Sacrificial silicon nano-structures were etched with XeF_2 to form nanochannels. Translocations of linearized DNA single molecules were imaged by fluorescence microscopy. Our method offers a manufacturable wafer-scale approach for CMOS-compatible bio-chips.

9:30 a.m.
14.2 CMOS Based High Density Micro Array Platform for Electrochemical Detection and Enumeration of Cells, C.C. Wong, C. Drews, Y. Chen, T.S. Pui, S.K. Arya, R. Weerasekera, A.R.A. Rahman, Institute of Microelectronics, A*STAR

Semiconductor electronic array technology has revolutionized in-vitro diagnostics in cellular manipulation and genomic research. The technology is advantageous as microbeads or cells within an enriched sample, can be controlled or detected in high-throughput manner. Here we present a highly sensitive label-free complementary-metal-oxide- semiconductor (CMOS) based high density micro-array for electrochemical detection and enumeration of breast tumor cell (MCF-7). The electrochemical impedance spectroscopy (EIS) based detection platform exhibited detection at single cell resolution (22 μm) and enumeration with mapping accuracy of ~80%. Maximum tumor-cell impedance increase of 28% was recorded. This platform has potential applications in clinical cancer diagnosis, such as identifying adherent tumor cells from the non-adherent white blood cells in enriched samples.

9:55 a.m.
14.3 A Novel Side-Gated Ultrathin-Channel Nanopore FET (SGNAFET) Sensor for Direct DNA Sequencing, I. Yanagi, T. Oura*, T. Haga, M. Ando, J. Yamamoto, T. Mine, T. Isida, T. Hatano, R. Akahori, T. Yokoi, T. Anazawa, Y. Goto, Hitachi, Ltd., *Hitachi High-Technologies Corporation

A side-gated ultrathin-channel nanopore FET (SGNAFET), for direct DNA sequencing with high resolution and sensitivity, is proposed. The goal of the SGNAFET is identifying each nucleotide by changes in channel current. A SGNAFET with channel thicknesses of 2-4 nm was successfully operated, and DNA translocations were detected through its nanopore.

10:20 a.m.
14.4 A Novel Optical Multiplexed, Label-Free Bio-Photonic-Sensor Realized on CMOS-Compatible Optoelectronic Integrated Circuit (OEIC) Platform, J. Song, X. Luo, J.S. Kee, Q. Liu, K.W. Kim, Y. Shin, M.K. Park, K.W. Ang, G. Lo, Institute of Microelectronics, A*STAR

We present novel electrical control and electrical directly readout on-chip optical label-free bio-sensing system. It comprises CMOS compatible OEICs and adopts low-cost broadband light source to facilitate hand-held-sized and cost-effective device for point-of-care applications. Label-free, multiplexed detection of DNA targets for pathogen bacteria with probe DNA modified sensor is demonstrated.

10:45 a.m.

14.5 A Novel SiNW/CMOS Hybrid Biosensor for High Sensitivity/Low Noise, J. Lee, S. Hwang, B. Choi, J.H. Lee*, B.-G. Park*, D.-I. Moon**, M.-L. Seol**, C.-H. Kim**, Y.-K. Choi**, D.M. Kim, D.H. Kim, S.-J. Choi, Kookmin University, *Seoul National University, **KAIST

A novel silicon nanowire (SiNW)/CMOS hybrid biosensor is demonstrated for the first time. It features a hybrid combination of a complementary SiNW block and CMOS logic inverter readout circuitry. The proposed hybrid biosensor shows remarkably sensitive output voltage (Δ1.2V/Δ0.4pH and Δ1.2V/Δ200fM DNA) without noise or fluctuation.

11:10 a.m.

14.6 Wafer-Scale Flexible Graphene Strain Sensors, H. Tian, Y. Shu, Y.-L. Cui, Y. Yang, D. Xie, Y. Zhang*, T.-L. Ren, Tsinghua University, *Lawrence Berkeley National Laboratory

In this paper, wafer-scale flexible strain sensors with high-performance are fabricated in one-step laser scribing. The graphene films could be obtained by direct reducing graphene oxide film in a Light-Scribe DVD burner. Our graphene strain sensor has the gauge factor (GF) of 0.11. In order to enhance the GF further, the graphene micro-ribbon has been used as strain sensors, which has the GF up to 9.49, which is higher than most of the reported that of graphene strain sensors (0.55~6.1). Our devices can meet the needs of specific applications, for example, high GF for low-strain applications and low GF for high deformation applications. Our work indicates that laser scribed flexible graphene strain sensors could be widely used for medical-sensing, bio-sensing, artificial skin and many other areas.

Session 15: Characterization, Reliability, and Yield – Reliability of BEOL and FEOL Devices: Breakdown and Instability

Tuesday, December 10, 9:00 a.m.

Columbia Rooms 6&8

Co-Chairs: Ahmad Ehteshamul Islam, Air Force Research Laboratory, WPAFB
Ernest Wu, IBM Corporation

9:05 a.m.

15.1 Reliability, Failure, and Fundamental Limits of Graphene and Nanotube Interconnects (Invited), A. Liao, A. Behnam, V. Dorgan, Z. Li, E. Pop, University of Illinois at Urbana-Champaign

Copper interconnects suffer from electromigration, grain boundary, and edge scattering at highly scaled technology nodes. In contrast, sp^2-hybridized carbon allotropes, such as graphene nanoribbons (GNRs) and carbon nanotubes (CNTs), could offer potential alternatives for next-generation interconnects without experiencing early failure from electromigration. Nevertheless, these materials come with their own sets of challenges, and many of their fundamental limitations are still not well understood. In this invited abstract we summarize several years of systematic efforts in examining graphene, GNRs, and metallic single-wall nanotubes (SWNTs) up to their extreme failure limits. We have found that reliability of SWNT and GNR interconnects depends fundamentally on their thermal dissipation rather than on electromigration as in Cu interconnects. To maximize reliability of nanoscale carbon conductors, the choice of dielectrics and thermal interfaces becomes crucial, in addition to continued efforts for higher quality materials with better intrinsic parameters.

9:30 a.m.

15.2 Understanding the Suppressed Charge Trapping in Relaxed- and Strained-Ge/SiO_2/HfO_2 pMOSFETs and Implications for the Screening of Alternative High-Mobility Substrate/Dielectric CMOS Gate Stacks, J. Franco, B. Kaczer, Ph. J. Roussel, J. Mitard, S. Sioncke, L. Witters, H. Mertens, T. Grasser*, G. Groeseneken, imec, *T.U. Wien

We propose a general model for understanding of charge-trapping in relaxed- and strained-Ge pMOS and nMOS with both standard SiO_2/HfO_2 and alternative GeOx-based high-k gate stacks. We introduce a universal metric to identify alternative substrate/dielectric systems with sufficient carrier-defect energy decoupling, necessary for achieving reliable high-mobility devices.

9:55 a.m.
15.3 A Time-Dependent Clustering Model for Non-Uniform Dielectric Breakdown, E. Wu, B. Li, J. Stathis, R. Achanta, IBM SRDC

We report a time-dependent clustering model for non-uniform dielectric breakdown for the first time. Its validity in terms of area transformations and percentile scaling properties has been rigorously investigated. We demonstrate its excellent agreement with multiple sets of experimental data of low-k, SiO_2, Si_3N_4, and high-k dielectrics in BEOL, MOL, and FEOL applications. We show its strong impact on reliability projection of clutering model in presence of multiple variabilities (or non-uniformities) in a dielectric system, particularly important for future technologies with extremely small dimensions.

10:20 a.m.
15.4 BTI Variability Fundamental Understandings and Impact on Digital Logic By the Use of Extensive Dataset, D. Angot, V. Huard, L. Rahhal, A. Cros, X. Federspiel, A. Bajolet, Y. Carmineti, M. Saliva, E. Pion, F. Cacho, A. Bravaix*, STMicroelectronics, *IM2NP-ISEN UMR

As a consequence of gate dielectrics scaling, NBTI degradation has emerged as dominant degradation mechanism for its average impact on product performance. At the same time, the continuous transistor dimensions reduction has led to an enlarged role of time-zero variability. More recently,pioneering works had paved the way towards the understanding of the role of NBTI variability. Though a general consensus starts emerging on the average NBTI modeling, the accurate theoretical description of NBTI variability is still under discussion. In spite of great achievements, the constant lack of statistics is one the main blocking point to solve out between various theoretical distributions. In this paper, we first describe the statistical distribution required for NBTI variability based upon an extensive dataset of more than 1 million transistors. In a second step, we propose a novel description approach for the NBTI-induced mismatch and how it depends on various process steps and compares with time-zero variability. Finally, the impact of such findings at device-level will be demonstrated to have extensions up to circuit-level.

10:45 a.m.
15.5 Hydrogen-Related Volatile Defects as the Possible Cause for the Recoverable Component of NBTI, T. Grasser, K. Rott*, H. Reisinger, M. Waltl, P.-J. Wagner, F. Schanovsky, W. Goes, G. Pobegen**, B. Kaczer***, TU Wien, *Infineon Munich, **KAI, ***IMEC

The recently suggested time-dependent defect spectroscopy (TDDS) has allowed us to study the recoverable component of NBTI at the single-defect level. To go beyond our previous efforts, we have performed a long-term TDDS study covering also the kilo-second time window. We found that even in this window NBTI recovery is due to a collection of first-order reactions. In particular, there is no trace of a diffusion-limited processes as assumed in the reaction-diffusion model. Most intriguingly, the responsible traps show various degrees of volatility, that is, they can disappear and reappear. Our observations lend strong support to the idea that NBTI recovery is due to hydrogen-related defects which are active when a H atom is at the defect site and inactive when not.

11:10 a.m.
15.6 Negative Bias Temperature Instability Lifetime Prediction: Problems and Solutions, Z. Ji, S.F.W. M. Hatta, J.F. Zhang, J.G. Ma, W. Zhang, N. Soin*, B. Kaczer**, S. De Gendt**, G. Groeseneken**, Liverpool John Moores University, *University of Malaya, **IMEC

NBTI lifetime is a figure-of-merit for process screening. The conventional DC-prediction overestimates lifetime due to recovery. The fast pulse method suppresses recovery, but does not give reliable prediction. This work proposes a new technique that overcomes the shortcomings of both DC and pulse methods and is readily implementable in industry.

Luncheon

Tuesday, December 10, 12:20 p.m.
Grand Ballroom West

Luncheon Presentation: *Graphics & GPU Computing: Past, Present, and Future*
David Luebke, Nvidia Corporation

The GPU, or Graphics Processing Unit, is the chip or IP block that powers the amazing visuals found in today's video games - visuals that compare in many ways to what we see in film. But modern GPUs have outgrown their graphics heritage in many ways to emerge as the world's most successful parallel computing architecture. The GPUs that consumers buy to play video games provide a level of massively parallel computation in a single chip that was once the preserve of supercomputers. The raw computational horsepower of these chips has expanded their reach well beyond graphics. Today's GPUs not only render video game frames, they also accelerate astrophysics, video transcoding, image processing, protein folding, seismic exploration, computational finance, radioastronomy, heart surgery, self-driving cars - the list goes on and on.

When thinking about the future of GPUs it is important to reflect on the past. How did this peripheral grow into a processing powerhouse found everywhere from medical clinics to radiotelescopes to supercomputers? Why the graphics card and not the modem, or the mouse? Have GPUs really outgrown graphics and will they thus evolve into pure HPC processors? (hint: no).

This talk is intended as a sort of "state of the union" for graphics and GPU computing. I'll briefly cover the dual heritage of GPUs, both in terms of supercomputing and the evolution of fixed function graphics pipelines. I'll dive into some architectural differences between GPUs and CPUs. I'll discuss "computational graphics", the evolution of graphics itself into a general-purpose computational problem, and how that impacts GPU design and GPU computing. I'll show lots of pretty pictures and videos. Finally I'll describe the important problems and research topics facing practitioners and researchers in both GPU computing and graphics.

Session 16: Power and Compound Semiconductor Devices – III-V Logic
Tuesday, December 10, 2:15 p.m.
International Ballroom Center
Co-Chairs: *Tim Ashley, University of Warwick*
Niamh Waldron, imec

2:20 p.m.
16.1 InAs N-MOSFETs with Record Performance of I_{on} = 600 µA/µm at I_{off} = 100 nA/µm (V_d = 0.5 V), S.W. Chang, X. Li*, R. Oxland, S.W. Wang, T. Vasen, C.H. Wang, R. Contreras-Geurrero**, K.K. Bhuwalka, G. Doornbos, M.C. Holland, G. Vellianitis, M.J.H. van Dal, B. Duriez, M. Edirisooriya**, J.S. Rojas-Ramirez**, P. Ramvall***, S. Thoms*, U. Peralagu*, C.H. Hsieh^, Y.S. Chang^, K.M. Yin^, L.-E. Wernersson***, R. Droopad**, I. Thayne*, M. Passlack, C.H. Diaz^, TSMC R&D Europe, *University of Glasgow, **Texas State University, ***Lund University, ^TSMC

Record setting InAs N-MOSFETs are reported, demonstrating performance better than state-of-the-art HEMTs. At 0.5V and fixed I_{off}=100nA/µm, I_{on}=601µA/µm is achieved in 10nm unstrained InAs channels with L_g=130nm, $g_{m,ext}$=2.7mS/µm and S=85mV/dec (DIBL=40mV/V). Measured mobility is 7100cm^2/Vs at n_s=6.7· 10^{12}cm^{-2}. Device simulations elucidate the performance potential of our III-V N-MOSFETs.

2:45 p.m.
16.2 A New Self-aligned Quantum-Well MOSFET Architecture Fabricated by a Scalable Tight Pitch Process, J. Lin, X. Zhao, T. Yu, D.A. Antoniadis, J.A. del Alamo, Massachusetts Institute of Technology

We have developed a new III-V self-aligned Quantum-Well MOSFET (QW-MOSFET) architecture that features a scalable highly conducting ledge over the channel access region. This enables both very tight pitch devices as well as well controlled ledge length. The ledge is fabricated through wet-etch free process. This architecture enables to balance performance and short-channel effects. In this manner, we demonstrate L_g=70 nm InAs MOSFETs with a ledge length of 5 nm that feature the highest gm of 2.7 mS/um. Separately, devices with L_ledge=70 nm yield the highest ON current of 410 uA/um. We also demonstrate a working MOSFETs with L_g = 20 nm with very tight metal contact spacing. Our tight pitch devices reveal for the first time the existence of off-state leakage (GIDL) in III-V MOSFETs.

3:10 p.m.
16.3 Sub-100 nm InGaAs Quantum-Well (QW) MOSFETs with Al_2O_3/HfO_2 (EOT < 1 nm) for Low-Power Logic Applications, T.-W. Kim, D.-H. Kim, D.H. Koh*, H.M. Kwon, R.H. Back, D. Veksler, C. Huffman, K. Matthews, S. Oktyabrsky**, A. Greene**, Y. Ohsawa***, A. Ko^, H. Nakajima***, M. Takahashi***, T. Nishizuka***, H. Ohtake***, S.K. Banerjee*, S.-H. Shin^, D.H. Ko, C. Kang, D. Gilmer, R.J.W. Hill, W. Maszara^^, C. Hobbs, P.D. Kirsch, SEMATECH, *UT-Austin, **CNSE, ***TEL, ^Yonsei University, ^^GLOBALFOUNDRIES

We have demonstrated tri-gate sub-100 nm $In_{0.53}Ga_{0.47}As$ QW MOSFETs with electrostatic immunity of S = 77 mV/dec., DIBL = 10 mV/V, together with excellent carrier transport of $g_{m,max}$ > 1.5 mS/µm, at V_{DS} = 0.5 V. To date, these results exhibit the best combination of $g_{m,max}$ and S in any III-V MOSFET.

3:35 p.m.
16.4 High Performance Sub-20-nm-Channel-Length Extremely-Thin Body InAs-on-Insulator Tri-Gate MOSFETs with High Short Channel Effect Immunity and V_{th} Tunability, S.-H. Kim, M. Yokoyama, R. Nakane, M. Ichikawa*, T. Osada*, M. Hata*, M. Takenaka,S. Takagi, The University of Tokyo, *Sumitomo Chemical Co. Ltd.

In this study, we investigate effects of vertical scaling and the tri-gate structure on electrical properties of ETB InAs-OI MOSFETs including SCEs control and effective mobility (μ_{eff}). Here, vertical scaling includes the scaling of the thickness of gate dielectric, MOS interface buffer layer and channel layer. We have found that, since combination of vertical scaling and the Tri-gate structure have a significant impact on μ_{eff} and SCEs control, the transistor structure is carefully designed on a basis of these properties. In addition, threshold voltage (V_{th}) tunability is quite important for static and dynamic power consumption control in advanced VLSI circuit design. It is not easy, however, to control V_{th} in a wide range for multi-gate MOSFETs such as tall FinFETs. Also, there has been no report on V_{th} control for scaled III-V MOSFETs. Here, the multi-gate MOSFETs based on ETB/ultrathin buried oxide (BOX) structures are promising for satisfying both stringent SCE immunity and V_{th} tunability through back bias voltage (V_B) control. Therefore, we examine the V_{th} tunability in the ETB InAs-OI tri-gate MOSFETs by back biasing through BOX. Finally, we demonstrate the operation of sub-20-nm-Lch InAs-OI Tri-gate MOSFETs with good SCEs control and large maximum G_m ($G_{m,max}$) of 2.1 mS/μm and the excellent V_{th} tuning behavior by applying V_B.

4:00 p.m.
16.5 Near Ballistic Sub-7 nm $In_{0.53}Ga_{0.47}As$ Junctionless FET Featuring 1 nm Extremely-Thin Channel and Raised S/D Structure, K.H. Goh, Y. Guo, X. Gong, G.-C. Liang, Y-C. Yeo, National University of Singapore

In this work, we report the realization of $In_{0.53}Ga_{0.47}As$ Junctionless FET (JLFET) with the shortest reported channel length LCH (6 nm) for any III-V transistors. The JLFET features a 1 nm-thick extremely-thin channel sandwiched between a 1 nm-thick InP cap and the InP substrate, and a heavily doped raised S/D structure. Peak transconductance Gm,peak of 1480 μS/μm at VDS = 0.7 V with an EOT of 2.5 nm and an ultra-low S/D resistance RSD of 165 Ω.μm were achieved. In addition, the ballistic behavior of sub-7 nm III-V transistors was experimentally investigated by using a novel extraction approach for the first time. The $In_{0.53}Ga_{0.47}As$ JLFET with LCH of 6 nm was demonstrated to have a mean free path (λ) of 27.2 nm and nearly ballistic transport with ballistic efficiency (B) of 0.82.

4:25 p.m.
16.6 Impact of the Channel Thickness on the Performance of Ultrathin InGaAs Channel MOSFET Devices, A. Alian, M.A. Pourghaderi, Y. Mols, M. Cantoro, T. Ivanov, N. Collaert, A. Thean, IMEC

InGaAs channel MOSFETs with channel thicknesses down to 3nm were studied. Thinner channels improve electrostatics (SS=77mV/dec), however, the mobility rapidly drops (110 cm^2/Vs). 8-band k.p simulations were conducted for accurate insight into the device operation. As also experimentally observed, simulations suggest that the accumulation capacitance increases for thinner channels. It was also found that the InP buffer response increases the electron effective mass as the channel becomes thinner. Based on this work, InGaAs channel thicknesses of 5nm and below hit severe performance issues.

Session 17 – FOCUS SESSION: Circuit and Device Interaction – Analog and Mixed Signal Circuit/Device Interactions
Tuesday, December 10, 2:15 p.m.
International Ballroom East
Co-Chairs: *Peter Rickert, Texas Instruments*
Shouhei Kousai, Toshiba Corp.

2:20 p.m.

17.1 Where Are We Going? Product Scaling in the System on Chip Era (Invited), G. Taylor, Intel Labs

The combination of increasing analog IP and shrinking process features create new challenges for SoCs. Process scaling is detrimental to analog circuit performance, while increased integration leads to more interaction between analog and digital circuits. This requires changes to the way analog circuits are designed and validated, making mixed signal and statistical design approaches essential.

2:45 p.m.
17.2 Impact of Layout at Advanced Technology Nodes on the Performance and Variation of Digital and Analog Figures of Merit (Invited), S. Saxena, C. Dolainsky, M. Lunenborg, J. Cheng, B. Yu, R. Vallishayee, D. Ciplickas, PDF Solutions, Inc.

Technology discontinuities introduced to maintain CMOS scaling have increased the sensitivity of transistor performance and variation to its layout and neighborhood. This paper describes an infrastructure for statistical characterization of these layout effects. The data obtained from this infrastructure illustrates the impact of layout on transistor figures of merit useful for analog and digital design.

3:10 p.m.
17.3 Impact of Multi-Gate Device Architectures on Digital and Analog Circuits and its Implications on System-On-Chip Technologies (Invited), A. Thean, P. Wambacq, J. Lee, M. Cho, A. Veloso, Y. Sasaki, T. Chiarella, K. Miyaguchi, B. Parvais, M. Garcia Bardon, P. Schuddinck, N. Horiguchi, M. Dehan, A. Mercha, G. Van Der Plas, N. Collaert, D. Verkest, M.S. Kim, imec, Vrije Universiteit Brussel

This paper reviews some important process aspects of aggressively downscaled FinFET technologies and their implications on digital and analog figures of merits (FOMs). The need to downscale device architectures to enhance digital transistor electrostatics and circuit density led to influences in parasitics, variability, and noise, which impact analog FOMs. Therefore, it is important to understand the trade-offs due to the new devices and the upcoming process solutions to address them. Process features, variability and parasitics relevant to 14nm and beyond FinFET will be reviewed and their System-On-Chip (SOC) implications will be discussed.

3:35 p.m.
17.4 Nanometer CMOS from a Mixed-Signal/RF Perspective (Invited), M. Wakayama, Broadcom Corporation

The demise of embedded mixed-signal and RF circuits has long been predicted. New architectures that leverage high-speed digital circuits and new circuit topologies that exploit the improved properties of advanced devices have continued the viability of high-performance and low-cost embedded mixed-signal and RF circuits. This paper reviews the long time success of past nanometer nodes, and shows the latest accomplishments for the specific case of RF Tuners.

4:00 p.m.
17.5 Challenges Toward Millimeter-wave and Terahertz CMOS Circuits Enhanced by Design Techniques (Invited), K. Okada, Tokyo Institute of Technology

This paper presents several design techniques for enhancing both active and passive device characteristics without any process modification, especially in the millimeter-wave frequency range. A 60-GHz 20-Gb/s wireless transceiver employing the techniques is also demonstrated in 65-nm CMOS.

4:25 p.m.
17.6 Power-Efficient Ultrahigh-Speed CMOS Wireless Communications in Terahertz Era (Invited), M. Fujishima, Hiroshima University

When trying to obtain the highest possible performance of a MOSFET, the MOSFET must be biased such that its highest fmax is realized. If, on the other hand, the power consumption is a great concern, one can opt for a reduced-fmax design. Power-efficient bias points can be found in the FP (frequency-power) plot. The power reduction thus achieved might more than compensate for the penalty of requiring more gain stages. We have successfully demonstrated 11-Gb/s wireless data transfer over a distance of 3 m with a CMOS 135-GHz transceiver based on this design. 10x power saving is expected in return for 75-GHz fmax reduction at the transistor level. Continued improvement of the device performance is thus essential for achieving the ultimate low-power high-speed wireless communication (such as 60-GHz wireless LAN) as well as the ultimate speed and frequency ("terahertz").

Session 18: Sensors, MEMS, and BioMEMS – Sensors, Resonators, and Microsystems
Tuesday, December 10, 2:15 p.m.
Georgetown Room
Co-Chairs: Dana Weinstein, MIT/Cornell University
Siavash Pourkamali, University of Texas, Dallas

2:20 p.m.
18.1 Acoustically-Engineered Multi-Port AlN-on-Silicon Resonators for Accurate Temperature Sensing, R. Tabrizian, F. Ayazi, Georgia Institute of Technology

This paper reports for the first time, on a novel silicon microresonator that is acoustically engineered to facilitate independent piezoelectric transduction of multiple energy-trapped high-Q resonance modes with large TCF difference and integer frequency ratios, while suppressing other spurious modes. Acoustic energy trapping in the central part of the resonator and far from the substrate obviates the need for narrow support tethers, facilitating integration of several isolated metallic electrodes on the thin-film piezoelectric transducer that are freely routed through wide anchors of the microstructure towards separate electrical ports. This enables the implementation of multiple electrically isolated oscillators using a single resonator, which can be used to generate small beat frequency with very high temperature sensitivity from an integer linear combination of multiple energy-trapped modes. Such a beat frequency can be used to provide accurate device-level temperature sensing. An AlN-on-Silicon microresonator prototype implemented based on this technique on low-resistivity substrate has two energy-trapped modes at 109 MHz and 218 MHz, with a large TCF difference of ~7 ppm/°C which are separately transduced through two isolated electrical ports. A small beat frequency (fb) extracted from a linear combination of these modes has a linear temperature characteristic over -20°C to 100°C with a large TCF of ~8300 ppm/°C.

2:45 p.m.
18.2 A High Order Mode 6.4GHz Ultra-High Sensitivity Nanoscale Surface Acoustic Wave Biosensor, H.L Cai, Y. Yang, C.R. Guo, C.J. Zhou, T.X. Ye, C. Wu, J. Liu, T.L. Ren, Tsinghua University

An ultra-high sensitivity nanoscale Surface Acoustic Wave (SAW) biosensor operated in high order mode for DNA sequences detection is proposed. Nanoscale interdigitals are fabricated on $LiNbO_3$ substrate to achieve a high quality factor of over 4000 at about 6.4GHz. The biosensor shows an excellent linear response to the target DNA in the range of 1ng/ml to 1μg/ml and the difference of hybridized single DNA base can be distinguished. An effective DNA immobilization on delay area increases the frequency shifts greatly, which also contributes to the high sensitivity of $6.7x10^{-16}g/cm^2/Hz$.

3:10 p.m.
18.3 HEMT-Based Readout of a Thickness-Mode AlGaN/GaN Resonator, A. Ansari, M. Rais-Zadeh, University of Michigan

This work reports on the first time demonstration of a thickness-mode resonant-body high electron mobility transistor (RB HEMT) with a Q of 250 at 4.23 GHz. The dependence of acoustic transconductance on the HEMT biasing condition is discussed in detail. Co-integrated with GaN ICs, the proposed RB-HEMT can offer all-GaN integrated nano/micro sensors and systems.

3:35 p.m.
18.4 Foundry-CMOS Integrated Oscillator Circuits Based on Ultra-low Power Ovenized CMOS-MEMS Resonators, M.-H. Li, C.-Y. Chen, C.-S. Li, C.-H. Chin, C.-C. Chen, S.-S. Li, National Tsing Hua University

An ovenized micromechanical oscillator comprised of a heater-embedded resonator and an interface circuit to enable ultra-low heater power of only 0.47mW and thermal stability of less than 1ppm/°C has been reported in a foundry CMOS-based fabrication platform. The oscillator phase noise comparable to state-of-the-art flexural-mode MEMS oscillators was also demonstrated.

4:00 p.m.
18.5 Scalable Sensing of Interconnect Current with Magnetic Tunnel Junctions Embedded in Cu Interconnects, T. Takenaga, Y. Tsuzaki, T. Furukawa, C. Yoshida, Y. Yamazaki, A. Hatada, M. Nakabayashi, Y. Iba, A. Takahashi, H. Noshiro, K. Tsunoda, M. Aoki, H. Fukumoto, T. Sugii, Low-power Electronics Association and Project (LEAP)

A current sensor that can be integrated in back-end-of-line in the CMOS process with MTJs is proposed and evaluated. We demonstrated current sensing in Cu wires and obtained a sensitivity of up to 4.2%/mA. Moreover, we confirmed that the combination of smaller MTJs and finer wires can suppress the effects of environmental magnetic fields.

4:25 p.m.
18.6 Demonstration of A Single-chip Integrated MEMS Tunable Laser with 48-nm Wavelength Range, J. Tao*^, H. Cai^, J. Wu**, A. Liu*, Y.D. Gu^, D.L. Kwong^, *Nanyang Technological University, ^Institute of Microelectronics/ A*STAR, **Beijing University of Posts and Telecommunications

This paper reports an on-chip semi-integrated miniature MEMS tunable laser which has a novel 3D micro-optical coupling system. In particular, an optical fibre acts as a rod lens for beam convergence in the vertical plane, while a deep-etched silicon parabolic mirror confines the light in the horizontal plane. Another blaze grating is a rotatable MEMS structure for wavelength selection and tuning. We propose such micro optical design for efficient optical coupling and side mode suppression. The obtained coupling efficiency is as high as 76.5%, which is much higher than typical value of 3%-50% of other MEMS tunable lasers. Meanwhile, compared with other hybrid-integrated tunable lasers, our proposed laser demonstrates fast tuning speed (~ 0.15 ms), compact size (3 mm × 3.2 mm), large tuning range (potential ~ 48.3 nm), and single-chip integration without the additional requirement of optical lenses components.

Session 19: Nano Device Technology – Nanosheet and Nanotube Technology
Tuesday, December 10, 2:15 p.m.
Jefferson Room
Co-Chairs: Alan Seabaugh, University of Notre Dame
Philip Feng, Case Western Reserve University

2:20 p.m.
19.1 Novel Logic Devices Based on 2D Crystal Semiconductors: Opportunities and Challenges (Invited), P. Zhao, W.-S. Hwang, E. Kim*, R. Feenstra^, G. Gu+, J. Kang^, K. Banerjee^, A. Seabaugh, G. (Huili) Xing, D. Jena, University of Notre Dame, *Samsung Advanced Institute of Technology, **Carnegie Mellon University, +University of Tennessee, ^University of California Santa Barbara

Two-dimensional crystal semiconductors such as graphene, BN, and the transition-metal dichalcogenides (TMDs) have emerged as attractive candidates for ultrascaled electronic devices. This work presents a few novel devices based on them.

2:45 p.m.
19.2 High-Performance Flexible Nanoelectronics: 2D Atomic Channel Materials for Low-Power Digital and High-Frequency Analog Devices, J. Lee, S. Chang, T.-J. Ha, H. Li, R. Ruoff, A. Dodabalapur, D. Akinwande, University of Texas - Austin

We report the state-of-the-art flexible devices based on graphene for RF transistors and large bandgap MoS_2 for low-power transistors. Our studies feature record mobility, frequency, strain, subthreshold slope, elucidation of the coupled electrical-mechanical properties including buckling which degrades the gate control, and integration of capping layers to afford robust devices.

3:10 p.m.
19.3 Graphene/Fluoropolymer Hybrid Materials with Enhancement of All Device Properties for Improved Field-Effect Transistors, T. Ha, J. Lee, L. Tao, I. Kholmanov, R. Ruoff, P. Rossky, D. Akinwande, A. Dodabalapur, The University of Texas at Austin

We report on substantial improvement of electronic characteristics of FETs based on CVD graphene, reduced graphene oxide, and molybdenum disulfide by interacting capping layers of appropriate amorphous or polycrystalline fluoropolymers. All the key device properties are improved including mobilities, on-off ratio, electron-hole transport symmetry, Dirac voltage, and impurity doping.

3:35 p.m.
19.4 High-Performance Few-Layer-MoS_2 Field-Effect-Transistor with Record Low Contact-Resistance, W. Liu, J. Kang, W. Cao, D. Sarkar, Y. Khatami, D. Jena* and K. Bannerjee, UC Santa Barbara, *Notre Dame University

Recently Molybdenum Disulphide (MoS_2) has emerged as a promising candidate for low-power digital applications. Compared to monolayer (1L) MoS_2, few-layer MoS_2 (FL-MoS_2) is attractive due to its higher density of states (DOS). However, there is a lack of comprehensive study on FL-MoS_2 field-effect-transistor (FET). In this paper, we report a high-performance FL-MoS_2 FET with record low contact resistance (0.8 KΩ.μm), that competes with the metal-silicon contacts in CMOS technology. The correlation of device performance and the number of MoS_2 layers is established to guide designing high performance FL-MoS_2 FET. Moreover, it is found that edge contact (metal contact to each edge of MoS_2 layers) plays a key role in the efficient electron injection from metal to MoS_2, which is confirmed by experiments as well as density functional theory (DFT) calculations. Moreover, top gated FL-MoS_2 FET is also demonstrated with a robust current saturation and high drive-current even without source/drain doping.

4:00 p.m.

19.5 Carrier Response in Band Gap and Multiband Transport in Bilayer Graphene Under the Ultra-High Displacement, K. Nagashio, K. Kanayama, T. Nishimura, A. Toriumi, The University of Tokyo

We demonstrate the ultra-high displacement (D) of ~8 V/nm (n=~4×10^{13} cm^{-2}) in bilayer graphene using the solid state Y_2O_3 top gate, which is reached only by the ion gating so far. The systematic comparison of I-V and C-V curves at high D elucidates that the carriers in bilayer graphene electrically communicate with trap sites within the band gap and that the filling of carriers in the high energy sub-bands results in the reduction of the conductivity due to the inter-band scattering.

4:25 p.m.
19.6 Gate-Controlled Schottky Barrier Modulation for Superior Photoresponse of MoS_2 Field Effect Transistor, H.-M. Li, D.-Y. Lee, M.-S. Choi, D.-S. Qu, X.-C. Liu, C.-H. Ra, W.J. Yoo Sungkyunkwan University

An ultrahigh photocurrent (PC) signal (over 17 times higher compared to the dark current) was achieved in a multi-layer MoS_2 field effect transistor (FET), owing to a gate-controlled MoS_2/Ti/Au Schottky barrier (SB) modulation which can suppress the electron drift in dark environment and promote the collection of photo-excited charge carriers in illuminating environment. The SB modulation was demonstrated to provide the great potential of MoS_2 for optoelectronic applications.

4:50 p.m.
19.7 Monolithic Three-Dimensional Integration of Carbon Nanotube FET Complementary Logic Circuits, H. Wei, M. Shulaker, H.-S. P. Wong, S. Mitra, Stanford University

By overcoming challenges from CNT imperfections, we experimentally demonstrate, for the first time, cascaded and fully-complementary CNFET monolithic 3D ICs, spanning up to 3 layers, yet using supply voltages all the way down to 0.2V.

5:15 p.m.
19.8 Carbon Nanotube Complementary Logic based on Erbium Contacts and Self-Assembled High Purity Solution Tubes, S.-J. Han, S. Oida, H. Park, J. Hannon, G. Tulevski, W. Haensch, IBM T.J. Watson Research Center

We demonstrate, for the first time, high-yield NFETs and PFETs as well as complementary logic gates built on CNT arrays assembled from the solution tubes. CNTs with high semiconducting purity are precisely placed onto designed locations. This approach serves as an important stepping stone for subsequent CNT logic technology development.

5:40 p.m.
19.9 High-Performance Multi-Stage Graphene RF Receiver Integrated Circuit (Late News), S-J. Han, A. Valdes Garcia, S. Oida, K.A. Jenkins, W. Haensch, IBM T.J. Watson Research Center

We present the first multi-stage graphene integrated circuit using a novel fabrication method which fully preserves transistor quality. The circuit operates as an RF receiver front-end performing signal amplification, filtering, and down-conversion mixing. All passive and active components are fully integrated into 0.6 mm^2 area and fabricated on 200 *mm* Si wafers. The record high performance allows us to use the graphene integrated circuit to receive and restore digital text transmitted on a 4.3 GHz carrier signal– a routine function executed in modern wireless communication.

Session 20: Process and Manufacturing Technology – Fully Depleted Planar, 3D Ge Device Technology and RRAM Memory
Tuesday, December 10, 2:15 p.m.
Lincoln Room
Co-Chairs: *Jeff Xu, Qualcomm Technologies, Inc.*
Dina Triyoso, GLOBALFOUNDRIES

2:20 p.m.
20.1 Scaled p-channel Ge FinFET with Optimized Gate Stack and Record Performance Integrated on 300mm Si Wafers, B. Duriez, G. Vellianitis, M.J.H. van Dal, G. Doornbos, R. Oxland, K.K. Bhuwalka, M. Holland, Y.S. Chang, C.H. Hsieh, K.M. Yin, Y.C. See, M. Passlack, C.H. Diaz, TSMC

We demonstrate scaled high-k/metal gate p-channel Ge FinFETs integrated onto 300mm Si wafers for which the best device shows record peak g_{m},ext=2.7mS/µm and I_{on}=497µA/µm at I_{off}=100nA/µm, all at V_{ds}=-0.5V. The high performance is a result of successful integration of <110> oriented, highly scaled Ge fins on silicon substrates and of a low D_{it} gate stack with capacitance equivalent thickness (CET)=8Å.

2:45 p.m.
20.2 Density Scaling with Gate-All-Around Silicon Nanowire MOSFETs for the 10 nm Node and Beyond, S. Bangsaruntip, K. Balakrishnan, S.-L. Cheng, J. Chang, M. Brink, I. Lauer, L.M. Gignac, R. L. Bruce, S.U. Engelmann, A. Pyzyna, G.M. Cohen, C. Breslin, J.S. Newbury, D. Klaus, A. Majumdar, J.W. Sleight, M.A. Guillorn, IBM Research Division, T. J. Watson Research Center

We present gate-all-around silicon nanowire MOSFETs fabricated using a process capable of achieving a SiNW pitch of 30nm and a gate pitch of 60nm. We demonstrate for the first time densities commensurate with the 10nm node. This work achieves the highest SiNW performance at a gate pitch below 100nm.

3:10 p.m.
20.3 Gate-Last Integration on Planar FDSOI MOSFET: Impact of Mechanical Boosters and Channel Orientations, S. Morvan, C. Le Royer, F. Andrieu, P. Perreau, Y. Morand*, D. Cooper, M. Cassé, X. Garros, J.M. Hartmann, L. Tosti, L. Brévard, F. Ponthenier, M. Rivoire*, C. Euvrard, A. Seignard, P. Besson*, P. Caubet*, C. Leroux, R. Gassilloud, S. Bilel*, F. Allain, C. Tabone, T. Poiroux, O. Faynot, CEA-LETI, *STMicroelectronics

We present for the first time Gate-Last (GL) planar Fully Depleted (FD) SOI MOSFETs featuring both ultra thin silicon body (3-5nm) and BOX (25nm). Transistors with metal-last on high-k first (TiN/HfSiON) have been successfully fabricated down to 15nm gate length. We have thoroughly characterized the gate stack (reliability, work-function tuning on Equivalent Oxide Thickness EOT=0.85nm) and transport (hole mobility, R_{access}) for different surface and channel orientations. We report excellent $I_{ON,p}$=1020µA/µm at I_{OFF},p=100nA/µm at V_{DD}=0.9V supply voltage for <110> pMOS channel on (001) surface with *in-situ* boron doped SiGe Raised Source and Drain (RSD) and compressive CESL. This is explained by the high efficiency of the strain transfer into the ultra-thin channel, as evidenced by physical strain measurements by dark field holography.

3:35 p.m.
20.4 Strained Germanium Quantum Well pMOS FinFETs Fabricated on *in-situ* Phosphorus-Doped SiGe Strain Relaxed Buffer Layers Using a Replacement Fin Process, L. Witters, J. Mitard, R. Loo, G. Eneman, H. Mertens, D.P. Brunco*, S.H. Lee**, N. Waldron, A. Hikavyy, P. Favia, A.P. Milenin, Y. Shimura, C. Vrancken, H. Bender, N. Horiguchi, K. Barla, A. Thean, N. Collaert, imec, *GLOBALFOUNDRIES, **Samsung

Strained Ge p-channel FinFETs on Strain Relaxed SiGe using a Fin replacement process are reported for the first time, demonstrating peak transconductance gm_{SAT} values of 1.3mS/um at V_{DS}=-0.5V and good short channel control down to 60nm gate length. Optimization of P-doping in the SiGe, optimized Si cap passivation thickness on the Ge, and improved gate wrap of the channel all improve device characteristics. The Ge FinFETs presented in this work outperform published relaxed Ge FinFET devices for the gm_{SAT}/SS_{SAT} benchmarking metric.

4:00 p.m.
20.5 Heated Ion Implantation Technology for Highly Reliable Metal-gate/High-k CMOS SOI FinFETs, W. Mizubayashi, H. Onoda*, Y. Nakashima*, Y. Ishikawa, T. Matsukawa, K. Endo, Y. X. Liu, S. O'uchi, J. Tsukada, H. Yamauchi, S. Migita, Y. Morita, H. Ota, M. Masahara, AIST, *Nissin Ion Equipment Co., Ltd.

The impact of the heated ion implantation (I/I) technology on metal-gate(MG)/high-k(HK) CMOS SOI FinFET performance and reliability has thoroughly been investigated. It was demonstrated that the heated I/I brings perfect crystallization after annealing even in ultrathin Si channel. For the first time, it was found that the heated I/I dramatically improves the characteristics such as I_{on}-I_{off}, Vth variability, and bias temperature instability (BTI) for both nMOS and pMOS FinFETs in comparison with conventional room temperature I/I.

4:25 p.m.
20.6 Improved Sidewall Doping of Extensions by AsH_3 Ion Assisted Deposition and Doping (IADD) with Small Implant Angle for Scaled NMOS Si Bulk FinFETs, Y. Sasaki, L. Godet*, T. Chiarella, D. P. Brunco**, T. Rockwell*, J. W. Lee, B. Colombeau*, M. Togo, S. A. Chew, G. Zschaetszch, K.B. Noh***, A. De Keersgieter, G. Boccardi, M. S. Kim, G. Hellings, P. Martin*, W. Vandervorst, A. Thean, N. Horiguchi, imec, *Applied Materials, **GLOBALFOUNDRIES, ***SK-Hynix

We demonstrate a novel photoresist-compatible FinFET doping, Ion Assisted Deposition and Doping, that combines the advantages of deposition and implantation. Energy and deposition thickness optimization reduces external resistance. On current is improved by 6-8% for L_G=26-30 nm and by 15% for L_G=20 nm, with better SCE and DIBL.

4:50 p.m.
20.7 A Low-cost, Forming-free WO_x ReRAM Using Novel Self-aligned Photo-Induced Oxidation, F.-M. Lee, Y.-Y. Lin, W.-C. Chien, E.-K. Lai*, D.-Y. Lee, C.-C. Yu, H.-H. Hsu, M.-H. Lee, H.-L. Lung, K.-Y. Hsieh, C.-Y. Lu, Macronix International Co., Ltd., *National Tsing Hua University

A novel CMOS compatible photo oxidation (PO) technology is proposed in this paper which, by only using standard DUV photo lithography process, demonstrates a strong oxidation capability to form CMOS compatible WOx. The oxidation occurs through catalytic chemical reaction during the post exposure baking (PEB) process. Based on this unique PO process, a high performance forming free 1T-1R WOx ReRAM is demonstrated. Furthermore, this PO WOx ReRAM can withstand high temperature baking (@250°C) for 30min thus is suitable for embedded systems that require pre-coding, and automotive and other industrial applications.

5:15 p.m.
20.8 First Demonstration of RRAM Patterned by Block Copolymer Self-Assembly, Y. Wu, H. Yi, Z. Zhang, Z. Jiang, J. Sohn, S. Wong, H.-S. P Wong, Stanford University

We report the first metal oxide RRAM device using diblock copolymer self-assembly lithography patterning and successfully scale down the memory device to less than 12 nm. The fabricated bi-layer TiOx/HfOx devices show excellent performance: low forming voltages (~2.5 V) and low switching voltages (<1.5 V); good cycle-to-cycle and device-to-device uniformities, reasonable endurance (>1E7 cycles) and retention property (>4E4 s @125^{o}C). Furthermore, self-assembly patterned single-layer HfOx-based RRAM devices is demonstrated with faster switching speed (~50 ns), multi-level storage (2 bits/cell), longer endurance (>1E9 cycles), half-selected read immunity (~1E9 cycles), good retention (>1E5s @125^{o}C).

Session 21: Characterization, Reliability, and Yield – Memory Characterization and Reliability
Tuesday, December 10, 2:15 p.m.
Columbia Rooms 5&7
Co-Chairs: *Eric Vogel, Georgia Institute of Technology*
Wen-Jer Tsai, Macronix

2:20 p.m.
21.1 Stochastic Variability of Vacancy Filament Configuration in Ultra-Thin Dielectric RRAM and its Impact on OFF-State Reliability, N. Raghavan, R. Degraeve, A. Fantini, L. Goux, D. Wouters, G. Groeseneken, M. Jurczak, IMEC / Katholieke Universiteit Leuven (KUL), IMEC

Considering SET and RESET to be dynamic stochastic processes involving the generation-recombination and drift-diffusion of multiple oxygen ions / vacancies, we examine the microscopic statistical changes in the shape of the filament during multiple switching cycles in ultra-thin low-power HfOx-based RRAM and evaluate the effect of forming compliance, dielectric microstructure, multi-layer dielectric films and Al-doping on the variability in the filament geometry, governed by two defect energy band frequency factors, ωX and ωY, based on the quantum point contact (QPC) formulation. The stability (reliability) of the filament in the OFF-state to non-equilibrium vacancy-induced perturbations is evaluated using the disturb voltage (VDIST) as a quantitative criterion during slow ramped voltage sweep. Microscopic changes of the defect arrangement in the OFF-state have a big influence on the filament stability. Operational, material and process design options are explored that can help enhance reliability (increase VDIST) of the OFF state. Moreover, the typical resistance level at which the filament undergoes "rupture" is documented for HfOx dielectric. The final configuration of the filament in the OFF-state is bimodal with a finite non-zero probability of being in the QPC mode or entering the tunnel barrier (TUN) mode.

2:45 p.m.
21.2 Characterizing Grain Size and Defect Energy Distribution in Vertical SONOS Poly-Si Channels by Means of a Resistive Network Model, R. Degraeve, M. Toledano-Luque, A. Arreghini, B. Tang, E. Capogreco, J. Lisoni, Ph. Roussel, B. Kaczer, G. Van den bosch, G. Groeseneken*, J. Van Houdt, imec, *KU Leuven

We demonstrate a resistive network model for poly-Si channel conduction that allows to reliably extract the poly-Si grain size and the energy distribution of the poly-Si defects from ISD-VG characteristics only. The model shows the separated impact of interface states and poly-Si states on current and Vth.

3:10 p.m.
21.3 Statistical Spectroscopy of Switching Traps in Deeply Scaled Vertical Poly-Si Channel for 3D Memories, M. Toledano-Luque, R. Degraeve, Ph. Roussel, V. Luong, B. Tang*, J.G. Lisoni, C.L. Tan, A. Arreghini, G. Van den bosch, G. Groeseneken, J. Van Houdt, imec, *Liverpool John Moores University

For future high density storage memories, 3D vertical poly-Si channel SONOS devices are emerging as the most prominent alternative due to the extreme reduction of cost per bit. However, this architecture faces RTN effects related to the highly defective channel that. These events potentially cause read errors during memory operation. The present abstract therefore aims at characterizing these adverse traps to gain insight into their physical properties. A statistical comparison among different polysilicon channels will be presented and benchmarked against monocrystalline planar nFETs, revealing that a significant part of the switching traps are placed in the poly-Si channel.

3:35 p.m.
21.4 Hot Atom Damage (HAD) Limited TDDB Lifetime of Ferroelectric Memories, M. Masuduzzaman, M. Alam, Purdue University

The AC/DC dielectric lifetime (TDDB) and failure distribution of ferroelectric materials have traditionally been characterized and interpreted similar to a classical gate oxide [1-3]. In this paper, we demonstrate the emergence of a fundamentally new kinetic pathway involving hot atom damage (HAD) in ferroelectrics, to interpret the severe reduction of AC lifetime (Fig. 3,7,8), coupled with a counterintuitive, sharp increase in the Weibull slope (Fig 9). Beyond a critical operating condition, the atoms are heated by the AC field, as they shuttle across the double-well energy landscape of the memory material (Figs. 5-9). An elegantly simple analytical model (i) interprets the existing experiments quantitatively (Fig 10), (ii) suggests strategies (e.g. pulse shaping) to minimize HAD significantly (Fig. 12) and (iii) predicts device lifetime at arbitrary operating conditions correctly (Fig. 13).

4:00 p.m.
21.5 Trade-off Between SET and Data Retention Performance Thanks to Innovative Materials for Phase-Change Memory, G. Navarro, M. Coué, A. Kiouseloglou, P. Noé, F. Fillot, V. Delaye, A. Persico, M. Bernard, C. Sabbione, D. Blachier, V. Sousa, L. Perniola, S. Maitrejean, A. Cabrini*, G. Torelli*, P. Zuliani**, R. Annunziata**, E. Palumbo**, M. Borghi**, G. Reimbold, B. De Salvo, CEA LETI MINATEC Campus, *University of Pavia, **STMicroelectronics

In this paper, for the first time, a focus on the trade-off between SET stability and RESET high-temperature data retention (HTDR) is proposed in N- or C-doped Ge-rich $Ge_2Sb_2Te_5$ based materials for Phase-Change Memories (PCM). Through physico-chemical analysis and electrical characterization we demonstrate the need for a specific "programming-current-vs-time-profile" to finally achieve a SET state stable at high-working temperature with programming times compatible with industrial applications. The reliability of the RESET and the SET states obtained with our optimized programming procedure has been demonstrated, which fully enables PCM for embedded applications.

4:25 p.m.
21.6 Conductive-AFM Tomography for 3D Filament Observation in Resistive Switching Devices, U. Celano, L. Goux, A. Belmonte, A. Schulze, K. Opsomer, C. Detavernier*, O. Richard, H. Bender, M. Jurczak, W. Vandervorst, imec, *University of Gent

In this paper, for the first time, we unveil the 3D-structure of a conductive filament (CF) for a scaled 1T1R CBAM memory element using C-AFM tomography. We present a new sub-nm resolved characterization technique (C-AFM tomography) enabling the 3D observation of nano-sized conductive features. We demonstrate the application of this concept by imaging the conductive filament for a functional device as well as for a device stuck in its low resistive state (LRS).

4:50 p.m.

21.7 Intrinsic Retention Statistics in Phase Change Memory (PCM) Arrays (Late News), M. Rizzi, N. Ciocchini, A. Montefiori*, M. Ferro**, P. Fantini**, A.L. Lacaita, D. Ielimini, Politecnico di Milano and IU.NET, *Università degli Studi di Milano-Biocca, **Micron

This work studies crystallization statistics in 1 Gb arrays of PCM devices. We evidence retention stabilization by tuning of the programming conditions, and erratic retention due to crystallization variability. A new retention model is developed, which is capable of predicting cell-to-cell and cycle-to-cycle variability as a function of programming conditions.

Session 22: Modeling and Simulation – Modeling and Simulation of Innovative Devices
Tuesday, December 10, 2:15 p.m.
Columbia Rooms 6 & 8
Co-Chairs: Luca Larcher, University of Modena and Reggio Emilia
Dmitry Veksler, SEMATECH

2:20 p.m.
22.1 Unified Reliability Modeling of Ge-Rich Phase Change Memory for Embedded Applications, N. Ciocchini, E. Palumbo*, M. Borghi*, P. Zuliani*, R. Annunziata*, D. Ielmini, Politecnico di Milano, *STMicroelectronics

This work addresses reliability of PCM based on Ge-rich GeSbTe. We evidence resistance drift and decay in the set state for the first time, which is attributed to grain-boundary relaxation and grain growth. A unified model is presented, capable of predicting the reliability of set/reset states at elevated temperature T.

2:45 p.m.
22.2 Connecting Physical and Electrical Properties of Hafnia-Based RRAM, B. Butcher, G. Bersuker, D.C. Gilmer, L. Larcher**, A. Padovani**, L. Vandelli**, R. Geer*, P.D. Kirsch, SEMATECH, *University of Albany, **Universita di Modena e Reggio Emilia

Introduction: RRAM technology presents an attractive option for the embedded non-volatile memory systems if its variability (cycle-to-cycle and device-to-device) can be controlled. To optimize RRAM performance from the standpoint of both device structural properties and operation conditions we need to understand the physical processes responsible for electrical characteristics [1]. Causative connections between electrical measurements and physical properties can be established only by employing simulations, which explicitly consider the HfO_2-specific nature of RRAM characteristics (in particular, relative oxygen affinities, valence states of ions and vacancies, ions diffusivities, dielectric crystallinity, etc.). In this study, based on the earlier proposed physical model [1,2], we developed a simulation model, which, for the first time, provides a consistent explanation for all reported critical RRAM features including the role of O-deficiency for repeatable switching, relation between switching characteristics and dielectric morphology, the advantage of generating oxygen deficiency using the oxygen gettering process, etc. The model successfully reproduces, with no fitting parameters, the observed LRS and HRS trends with respect to dielectric stoichiometry, forming voltage, and amplitude and duration of the reset pulse. Simulation model: In order to describe the impact of the material properties and forming conditions on device operations, we developed a full 3D simulation model (see preliminary results in [3]), capable of accounting for the stochastic nature of the forming and reset processes. The device space is discretized into a 3D matrix of unit volumes characterized by a resistance value, which depends on the local stoichiometry at any given (simulation) moment. A statistical Monte-Carlo method has been developed which accounts for the local power dissipation, temperature-increase-with-current, and for the temperature/E-field-driven vacancy-ion pairs generation/ recombination and oxygen ion diffusion at every xyz position. The derived 3D potential and temperature maps are then used to re-calculate vacancy/ion

generation/diffusion rates. In this study, RRAM devices with the TiN/Ti/5nm HfO_2/TiN stacks and cell sizes of 20x20 nm^2 were simulated. Numerical values of all the material parameters used in the simulations were obtained from the published reports. In this set of simulations, after the device structure is defined (see Fig. 1 A1,2 - D1, D2), there are no fitting parameters.

3:10 p.m.
22.3 Atomic Migration in Phase Change Materials, G. Novielli, A. Ghetti, E. Varesi, A. Mauri, R. Sacco*, Micron Technology Inc., *Politecnico of Milan

We introduce a comprehensive 3D physical model for mass transport in PCM materials. In addition to the driving force for atom diffusion coming from concentration gradient and electric field, the model also accounts for the effect of temperature gradient and phase segregation. This new diffusion model is coupled with a calibrated electro-thermal-phase change model, thus providing a unified framework for the self-consistent simulation of both the electro-thermal and the phase/material change problems. The model is applied to the study of different types of PCM cells showing good agreement with experimental data and demonstrating in particular the fundamental role played by the temperature profile.

3:35 p.m.
22.4 Domain Wall Gate for Magnetic Logic and Memory Applications with Perpendicular Anisotropy, S. Breitkreutz, G. Ziemys, I. Eichwald, J. Kiermaier, G. Csaba*, W. Porod*, D. Schmitt-Landsiedel, M. Becherer, Technische Universität München, *University of Notre Dame

In this work, we experimentally demonstrate a novel device, where the domain wall propagation in a nanowire is locally controlled by surrounding magnets. The presented domain wall gate enables logic operation, can act as an on-off switch in magnetic interconnects and has far reaching applications in magneto-logic and magnetic memories.

4:00 p.m.
22.5 Analytic Model of Endurance Degradation and Its Practical Applications for Operation Scheme Optimization in Metal Oxide Based RRAM, P. Huang, B. Chen, B. Gao, Y. Wang, F. Zhang, L. Shen, L. Zeng, G. Du, X. Zhang, J. Kang, X. Liu, X. Wang, B.B. Weng, Y. Tang, G.Q. Lo, D.-L. Kwong, Peking University, IME*ASTAR

Key achievements: 1) Analytic model of endurance degradation is presented by further extending our previous model of RRAM transient operation. The endurance degradation behavior predicted by the developed model is verified by the published experimental data in different devices under various operation schemes; 2) Optimized operation scheme for multi-bit data storage is proposed based on the model prediction and 106 switching cycle of all the 4-level resistance states in HfOx based RRAM is achieved; 3) An innovative dynamic self-recovery operation scheme is proposed for high speed and robust endurance switching for the first time.

4:25 p.m.
22.6 Novel 3D Random-Network Model for Threshold Switching of Phase-Change Memories, E. Piccinini, A. Cappelli*, F. Xiong**, A. Behnam, F. Buscemi, R. Brunetti*, M. Rudan, E. Pop**, C. Jacoboni*, Università di Bologna, *Università di Modena e Reggio Emilia, **University of Illinois at Urbana-Champaign

We study the heat and charge transport and the Ovonic- and Memory-Threshold-Switching in PCM through a 3D random network model based on trap-limited conduction and coupled with electrothermal FEA. The model accurately describes experimental IV data featuring sudden crystallization voltage snap-back. The outcome of the simulations also allows us to microscopically correlate the onset of hot-carrier

preferential paths to Ovonic switching and to current-induced crystallization. Moreover, we statistically analyze multiple instances of the microscopic random network in order to provide an estimate of the variability of the device properties due to the intrinsic disorder.

Session 23: Evening Panel
Tuesday, December 10, 8:00 p.m.
International Ballroom Center

Is there life beyond conventional CMOS?

Moderator: Jeff Welser, IBM

For almost half a century, the ability to achieve increased performance per dollar in semiconductor chips by scaling the dimensions of the field-effect transistor (FET) in Complimentary Metal Oxide Semiconductor (CMOS) technology has been the driving engine behind the global semiconductor industry. However, in recent generations, exponentially increasing power density due to leakage currents as well as active switching energy of these nanoscale transistors is limiting our ability to reap the historical benefits of continued scaling. We are now forced to trade-off performance and/or density for reduced power consumption, and hence the fundamental physics of the CMOS transistor operation, rather than fabrication capability alone, are turning out to be an equally formidable limit for future scaling. Research focused on finding a new logic device that could show significant advantage over ultimate FETs in power, performance, density, and/or cost to enable the industry to extend the historical cost and performance scaling trends has begun in earnest. There are many contenders vying to be the "next switch" (TFET, CNT, GNR, Spintronic devices, BISFET, Nanomagnets, etc.), but so far most candidates – even if we could build them – are slower than CMOS, and consequently are not competitive in performance when building typical CMOS architectures based on Boolean logic gates. However, many show potential for much lower energy operation – which continues to be a primary limiter for any device to scale – as well as having unique functionality, such as non-volatility or reconfigurabilty. We may need to take better advantage of these properties by thinking beyond the logic device itself to the circuit and architecture level.

The panel will explore some key questions such as:

- What are the key technology limiters holding back future logic device contenders?
- Which device or class of devices shows the most promise for beating CMOS for high performance applications? Low power applications? Any applications?
- Do any devices or materials offer new capabilities or features that could augment CMOS technology for future nodes?
- Will we have to change the circuit architecture to match the new device? Will we stick with Boolean logic, or change the computation approach entirely?
- Does any device exhibit the potential for multi-generation scaling? Can we afford a device that just gives us one more node?

Panelists:

An Chen, GLOBALFOUNDRIES
Tetsuo Endoh, Tohoku University
Marc Heyns, IMEC Fellow
Mark Rodwell, UC Santa Barbara
Alan Seabaugh, University of Notre Dame
Ian Young, Intel

Session 24: Evening Panel
Tuesday, December 10, 8:00 p.m.
International Ballroom East

Will Voltage Scaling in CMOS Technology Continue Beyond 14nm Generation?

Moderator: Kevin Zhang, Intel

Voltage scaling has long been an essential and beneficial component in our pursuit of Moore's Law for CMOS technologies, to achieve ever-higher integration and more energy-efficient computing. Lower voltage operation has become even more important in today's power-constrained world, where mobile applications are fueling the future growth of the semiconductor industry. However, voltage scaling has encountered significant barriers in recent years as the feature size of CMOS devices has shrunk well below 50nm. The pace of voltage scaling has slowed, and the risk of voltage scaling coming to a halt is growing.

The panel will explore a wide range of topics associated with voltage scaling from both Technology and Design perspectives.

1. What are the fundamental technical challenges that limit voltage scaling in today's CMOS technologies?
2. What can circuit designers do to help further the voltage scaling in CMOS technologies?
3. What are the new transistor technologies on the horizon that could push the voltage scaling further downward?
4. What should Designers and Technologists do in a "post voltage scaling era" if voltage scaling reaches its limit?

Panelists:

Rob Aitken, ARM
Kelin Kuhn, Intel
Sreedhar Natarajan, TSMC
Tak Ning, IBM
An Steegen, IMEC
Nobuyuki Sugii, LEAP

Session 25: Circuit and Device Interaction – Advanced 3D Packaging and Emerging Memory Systems
Wednesday, December 11, 9:00 a.m.
International Ballroom West
Co-Chairs: Myunghee Na, IBM
Munehiro Tada, LEAP

9:05 a.m.
25.1 Array Antenna Integrated Fan-out Wafer Level Packaging (InFO-WLP) for Millimeter Wave System Applications, C.-H. Tsai, J.-S. Hsieh, H.-H. Chen, C.-W. Hsiao, C.-S. Chen, C.-S. Liu, M.-J. Lii, C.-T. Wang, D. Yu, TSMC

A high gain array antenna integrated fan-out wafer level technology is developed for millimeter wave system applications. A 4 x 4 array antenna on the fan-out structure with form factor of 10 x 10 x 0.5 mm3, gain of 16.4 dBi, and interconnect loss of 0.7 dB is achieved.

9:30 a.m.
25.2 3D Heterogeneous Integration for Analog (Invited), A. Samoilov, K. Tran, N. Kerness, J. Jones, P. McNally, S. Barnett, T. Parent, J. Ellul, A. Srivastava, K. Ikeuchi, T. Wang, T. Zhou, Maxim Integrated

We illustrate capabilities of 3D integration for analog applications through both wafer-level and packaging technologies. Examples of wafer-level 3D integration include integrated capacitors and optical sensors. Integrated Si capacitors demonstrate the highest reported capacitor density of C=1 $\mu F/mm^2$ and the figure of merit (FOM) $C*V_{bd}$=11 C/m^2 (V_{bd} is the breakdown voltage). Through-Si vias can be used to combine passive and active die into a single stack. Addition of optical layers to the Bipolar CMOS DMOS (BCD) process allows light detection in the visible and infrared range. 3D package-level integration is illustrated by embedding of multiple active and passive components in one package.

9:55 a.m.
25.3 Magnetic Wireless Interlayer Transmission Through Perpendicular MTJ for 3D-IC Applications, C.-H. Wang, K.-Y.Dai, K.-H. Shen*, Y.-H. Wang*, M.-J. Tsai*, C.-J. Lin, Y.-C. King, National Tsing-Hua University, *Industrial Technology Research Institute

A new wireless 3D IC connection method, Magnetic-sensing Transmission Interface (MTI), is reported, for the first time. MTI implemented by placing a high-sensitivity sensor with perpendicular magnetic anisotropy on the top of a micro-coil is successfully demonstrated. This new contactless connection scheme offers low-power, wide-bandwidth and multi-layer wireless data transmission for 3D ICs.

10:20 a.m.
25.4 Variable Nonvolatile Memory Arrays for Adaptive Computing Systems, H. Noguchi, S. Takeda, K. Nomura, K. Abe, K. Ikegami, E. Kitagawa, N. Shimomura, J. Ito, S. Fujita, Toshiba

This paper presents a novel computing circuit based on 1T-1MTJ of perpendicular STT-MRAM memory arrays. It can cover all memory hierarchy and computing units that are variable and adjustable to applications by selecting single, dual or quadruple cell mode and changing circuit resource.

10:45 a.m.
25.5 Experimental Demonstration of Array-level Learning with Phase Change Synaptic Devices, S.B. Eryilmaz, D. Kuzum*, R.G.D. Jeyasingh, S.B. Kim**, M. BrightSky**, C. Lam**, H.-S. Philip Wong, Stanford University, *University of Pennsylvania, **IBM Research, T.J. Watson Research Center

The computational performance of the biological brain has long attracted significant interest and has led to inspirations for computing and signal processing. In this work, we demonstrate, in hardware, that 2-D crossbar arrays of phase change synaptic devices can achieve associative learning and perform pattern recognition. Pattern recognition is robust against synaptic resistance variations and large variations can be tolerated by increasing the number of training iterations.

11:10 a.m.
25.6 Neuromorphic Speech Systems Using Advanced ReRAM-Based Synapse, S. Park, A.M. Sheri, J. Kim, J. Noh, J.-W. Jang*, M. Jeon, B.-G. Lee, B.H. Lee, B.H. Lee, H. Hwang*, Gwangju Institute of Science and Technology, *Pohang University of Science and Technology

We demonstrate an advanced ReRAM based analog artificial synapse for neuromorphic systems. Nitrogen doped TiN/PCMO based artificial synapse is proposed to improve the performance and reliability of the neuromorphic systems by using simple identical spikes. For the first time, we develop fully unsupervised learning with proposed analog synapses which is illustrated with the help of auditory and electroencephalography (EEG) applications.

11:35 a.m.
25.7 Design and Optimization Methodology for 3D RRAM Arrays, Y. Deng, H. -Y. Chen*, B. Gao, S. Yu*, S.-C Wu*, L. Zhao*, B. Chen, Z. Jiang*, T.-H Hou**, Y. Nishi*, J. Kang,H. -S. P Wong*, Peking University, *Stanford University, **National Chiao Tung University

3D RRAM arrays are studied at the device- and architecture- levels. The memory cell performance for a horizontal cross-point is shown experimentally to be essentially comparable to vertical pillar-around geometry. Array performances (read/write, energy, and speed) of different 3D architectures are investigated by SPICE simulation, showing horizontal stacked RRAM is superior but suffers from higher bit cost. Adopting a bi-layer pillar electrode structure is demonstrated to enlarge the array size in 3D vertical RRAM. The design guidelines are proposed for the 3D VRRAM: it shows that increasing the number of stacks of VRRAM while keeping the total bits the same, as well as scaling of feature size (F) are critical for reducing RC delay and energy consumption.

Session 26: Nano Device Technology – Ge Channel and Nanowire Devices
Wednesday, December 11, 9:00 a.m.
International Ballroom East
Co-Chairs: Witek Maszara, GLOBALFOUNDRIES
Ian Post, Intel

9:05 a.m.
26.1 High Mobility Strained-Ge pMOSFETs with 0.7-nm Ultrathin EOT Using Plasma Post Oxidation $HfO_2/Al_2O_3/GeO_x$ Gate Stacks and Strain Modulation, R. Zhang, W. Chern*, X. Yu, M. Takenaka, J.L. Hoyt*, S. Takagi, The University of Tokyo, *MIT Microsystems Technology Laboratories, Nanjing University

High mobility s-Ge pMOSFETs without Si passivation have been demonstrated using self-aligned NiGeSi metal S/D and $HfO_2/Al_2O_3/GeO_x$ gate stacks, formed by the plasma post oxidation method, with the thinnest EOT to date of 0.7 nm. Record high peak hole mobility of 763 cm^2/Vs has been achieved with 0.82 nm EOT, combined with the asymmetric compressive strain along <110> channel direction. These results suggest the feasibility of s-Ge pMOSFETs in future CMOS technology.

9:30 a.m.
26.2 Advantage of (001)/<100> Oriented Channels in Biaxially- and Uniaxially Strained-Ge-on-Insulator pMOSFETs with NiGe Metal Source/Drain, K Ikeda, Y. Moriyama, Y. Kamimuta, M. Ono, T. Irisawa, M. Oda, E. Kurosawa, T. Tezuka, National Institute of AIST

We compared current drivability between (001)/<100> and (001)/<110> strained Ge-on-insulator pMOSFETs under biaxial and uniaxial stress. Higher intrinsic transconductance ($g_{m,int}$) was experimentally demonstrated for the first time in the devices with a gate length (L_g) less than 100nm under the both condition, although this is not the case for the long-channel devices. This is possibly attributable to more significant non-parabolicity of the valence band (VB) dispersion, i.e., heavier effective mass at energy apart from the VB minimum, along <110> than along <100>. It is also found that the parasitic resistance (R_{SD}) governed by the contact resistance between the NiGe-source and the strained-Ge channel is lower along <100> direction than the counterpart. As a result, higher drive current of 644 μA/μm and 536 μA/μm at Vd =-0.5V were obtained for <100> devices with L_g of 55 nm both under the biaxial- and uniaxial strain, respectively.

9:55 a.m.
26.3 A Group IV Solution for 7nm FinFET CMOS: Stress Engineering Using Si, Ge and Sn, S. Gupta, V. Moroz*, L. Smith*, Q. Lu*, K. Saraswat, Stanford University, *Synopsys

In this work, we present a FinFET-based CMOS solution using group IV elements and alloys for device dimensions expected in a 7nm technology node. We find that inclusion of Sn-based alloys – GeSn and SiGeSn significantly expands the design space for continued band gap and stress engineering in a Si-compatible platform. In our design, we leverage the use of a common buffer layer for n and p channel devices to alleviate difficulties in integration of different channel materials. CMOS performance is evaluated through a detailed simulation study. Some of the critical challenges in realizing the proposed CMOS design are also investigated through experimental methods.

10:20 a.m.
26.4 FDSOI Nanowires: An Opportunity for Hybrid Circuit with Field Effect and Single Electron Transistors (Invited), M. Vinet, V. Deshpande, X. Jehl, R. Wacquez, S. Barraud, M. Sanquer, R. Coquand, O. Cueto, B. Roche, B. Voisin, M. Pierre, C. Vizioz, L. Tosti, B. Previtali, P. Perreau, T. Poiroux, O. Faynot, CEA-LETI, CEA-INAC

The paper summarizes our recent results showing that thanks to a well controlled CMOS FDSOI technology we have been able to demonstrate breakthroughs in the combined use of field effect and Coulomb blockade phenomena. On one hand, we have demonstrated room temperature hybrid circuits based on single electron transistors and MOSFETs. On the other hand, we have shown the practical performance of electron pumps designed with a single silicided Coulomb island and MOSFETs as tunable barriers for metrologic applications.

10:45 a.m.
26.5 A Practical Si Nanowire Technology with Nanowire-on-Insulator Structure for Beyond 10nm Logic Technologies, S.-G. Hur, J.-G. Yang, S.-S. Kim, D.-K. Lee, T. An, K.-J . Nam, S.-J. Kim, Z. Wu, W. Lee, U. Kwon, K.-H. Lee, Y. Park, W. Yang, J. Choi, H.-K. Kang, E.S. Jung, Samsung Electronics Co.

Si NW NMOSFET with 0.9nm EOT of Gox and LG of 24nm have been experimentally demonstrated. 13nm DNW showed the best I_{ON}-I_{OFF} performance by the lowest R_{EXT}, R_{CH} and the reduced GIDL current. With Nanowire-On-Insulator (NOI) structure, AC performance was improved by 20% at triple-NWs.

Furthermore, reliability was comparable with existing FinFET structure. Thus, it holds one of practical candidates for beyond 10nm device.

11:10 a.m.
26.6 Asymetrically Strained High Performance Germanium Gate-All-Around Nanowire p-FETs Featuring 3.5 nm Wire Width and Contractable Phase Change Liner Stressor ($Ge_2Sb_2Te_5$), R. Cheng, B. Liu, P. Guo, Y. Yang, Q. Zhou, X. Gong, D. Yuan, Y. Tong, K. Bourdelle*, N. Daval*, D. Delprat*, B.-Y. Nguyen*, Y.-C. Yeo, National University of Singapore

We report the first demonstration of Ge gate-all-around (GAA) nanowire (NW) p-FETs integrated with a contractable liner stressor. High performance GAA NW p-FET featuring the smallest wire width WNW of ~3.5 nm was fabricated. Peak intrinsic G_m of 581 μS/μm and SS of 125 mV/dec was demonstrated. When the Ge NW p-FETs were integrated with the phase change material $Ge_2Sb_2Te_5$ (GST) as a liner stressor, the high asymmetric strain was induced in the channel to boost the hole mobility, leading to ~95% intrinsic $G_{m,lin}$ and ~34% $G_{m,sat}$ enhancement. Strain and mobility simulations show good scalability of GST liner stressor and great potential for hole mobility enhancement.

11:35 a.m.
26.7 High Performance Ge CMOS with Novel InAIP-Passivated Channels for Future Sub-10 nm Technology Node Applications (Late News), B. Liu, X. Gong, R. Cheng, P. Guo, Q. Zhou, M. Hon, S. Owen, C. Guo, L. Wang, W. Wang, Y. Yang, Y-C. Yeo, C-T. Wan*, S-H. Chen*, C-C. Cheng*, Y.-R. Lin*, C.-H. Wu*, C-H. Ko*, C.H. Wann*, National University of Singapore, *Taiwan Semiconductor Manufacturing Company

A new InAlP passivation technology with large band offsets is demonstrated for Ge CMOS. Record high mobility of ~958 $cm^2/V•s$ at NINV of $6x10^{11}$ cm^{-2} was achieved for GE(100) nFETs, and a high peak hole mobility of ~390 $cm^2/V•s$ was obtained for Ge(100) p-FETs. Ge N-FinFETs were also fabricated.

Session 27: Display and Imaging Systems – Display and Imaging Devices
Wednesday, December 11, 9:00 a.m.
Georgetown Room
Co-Chairs: Daping Chu, University of Cambridge
Piet De Moor, imec

9:05 a.m.
27.1 High Performance Gallium-Zinc Oxynitride Thin Film Transistors For Next-Generation Display Applications, T.S. Kim, H.S. Kim, J.S. Park, K.S. Son, E.S. Kim, J.B. Seon, S. Lee, S.J. Seo, S.J. Kim, S. Jun*, K.M. Lee*, D.J. Shin*, J. Lee*, C. Jo*, S.J. Choi*, D.M. Kim*, D.H. Kim, M. Ryu, S.H. Cho, Y. Park, Samsung Advanced Institute of Technology, *Kookmin University

We present results from both experiment and first principle calculation showing that by controlling the amount of nitrogen and oxygen within the ZnON film and adding suitable dopant such as Ga, the TFT performance can be greatly improved to be applicable for next-generation TV backplanes.

9:30 a.m.
27.2 High Stability Fluorinated Zinc Oxide Thin Film Transistor And Its Application On High Precision Active-Matrix Touch Panel, Z. Ye, M. Wong*, M.-T. Ng*, J.K. Luo, Zhejiang University, *The Hong Kong University of Science and Technology

Implanted and plasma fluorinated zinc oxide TFTs was fabricated. The F-ZnO TFTs exhibit high mobility (~71 cm^2/Vs), good uniformity, light insensitivity and stable operation performance, due to the F

passivation effect in ZnO. A novel active-mactrix self-capacitive touch panel based on the F-ZnO TFTs was realized, which exhibits high precise handwriting input and sensitive multi-touch function.

9:55 a.m.
27.3 High Performance Amorphous Metal-Oxide Semiconductors Thin-Film Passive and Active Pixel Sensors, R. Zhang, L. Bie, T.-C.Fung*, J. Kanicki, University of Michigan, *Qualcomm MEMS Technologies, Inc.

In this paper, for the first time, we report on high performance a-IGZO TFTs based passive pixel sensor (PPS) and active pixel sensor (APS) circuits. Experimental results show that single-TFT PPS with a pitch length of 50μm achieved a signal charge gain approaching to unity (Gain=0.93) under a fast readout time of 20μs and a dynamic range of 40dB. APS based on three a-IGZO TFTs established a high dynamic range, which is more than 60dB. In addition, 2-TFTs half active pixel sensor (H-APS) testing circuits are also used to investigate the voltage gain properties for APS in this work.

10:20 a.m.
27.4 Three-dimensional Structures for High Saturation Signals and Crosstalk Suppression in 1.20 μm Pixel Back-Illuminated CMOS Image Sensor, T. Shinohara, K. Watanabe, S. Arakawa, H. Kawashima, A. Kawashima, T. Abe, T. Yanagita, K. Ohta, Y. Inada, M. Onizuka, H. Nakayama, Y. Tateshita, T. Morikawa, K. Ohno, D. Sugimoto, S. Kadomura, T. Hirayama, Sony Semiconductor Corporation

We present three-dimensional structures, vertical transfer gate and buried shielding metal that can be applied to our latest 1/2.3" 1.20 um 20M pixels back-illuminated CMOS image sensor. New pixel design and process exhibited 60% higher saturation signals and 50% lower crosstalk without any degradation in white blemish and dark current.

10:45 a.m.
27.5 A Geiger Mode APD Fabricated in Standard 65nm CMOS Technology, E. Charbon, H.-J. Yoon, Y. Maruyama, Delft University of Technology, EPFL, on leave to the Jet Propulsion Laboratory

We present the first avalanche photodiode (APD) fabricated in standard 65nm CMOS technology, operating both in proportional and Geiger modes. The APD comprises a n+p-well junction surrounded by guard-ring; PDP is in the 350-750nm range, peaking at 450nm; DCR is 1.5kHz/μm^2, while afterpulsing is negligible and jitter is 235ps FWHM.

11:10 a.m.
27.6 A Trench Gate Photo Cell for Spectrometric Applications, T. Kautzsch, A. Sciré, K. Voigtlaender, Infineon Technologies Dresden GmbH

A new trench gate photo cell for spectrometric sensing is demonstrated. By combining a trench structure with a gradually doped base, a device with minimum foot print and excellent spectral resolution is achieved. It offers new opportunities for ambient light recognition of mobile devices and for medical applications.

Session 28: Power and Compound Semiconductor Devices – Next Generation Logic and Power
Wednesday, December 11, 9:00 a.m.
Lincoln Room
Co-Chairs: *Gilbert Dewey, Intel Corporation*
Keisuke Shinohara, HRL Laboratories

9:05 a.m.

28.1 High I_{on}/I_{off} and Low Subthreshold Slope Planar-Type InGaAs Tunnel FETs with Zn-Diffused Source Junctions, M. Noguchi, S. Kim, M. Yokoyama, O.Ichikawa*, T. Osada*, M. Hata*, M. Takenaka, S. Takagi, The University of Tokyo, *Sumitomo Chemical Co. Ltd.

We have demonstrated the successful operation of the planar-type InGaAs TFET with the source regions formed by the solid-phase Zn diffusion, for the first time. The record small S.S. of 64 mV/dec and large Ion/Ioff ratio over 6 orders as the planar-type III-V TFETs are demonstrated.

9:30 a.m.

28.2 Demonstration of $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ Near Broken-Gap Tunnel FET with I_{ON}=740μA/μm, G_M=700μS/μm and Gigahertz Switching Performance at V_{DS}=0.5V, R. Bijesh, H. Liu, H. Madan, D. Mohata, W. Li*, N. Nguyen*, D. Gundlach*, C. Richter*, J. Maier, K. Wang, T. Clark, J. Fastenau**, D. Loubychev**, W. Liu**, V. Narayanan, S. Datta, Penn State University, *National Institute of Standards and Technology, **IQE, Inc.

We demonstrate high frequency switching characteristics of TFETs based on the $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ material system. These near broken-gap TFETs (NBTFETs) with 200nm channel length exhibit record drive current (I_{ON}) of 740μA/μm, intrinsic RF transconductance (GM) of 700μS/μm, and a cut-off frequency (FT) of 19 GHz at VDS=0.5V. Numerical simulations calibrated to the experimental data provide insight into the impact of vertical architecture on switching performance of TFETs at scaled technology nodes.

9:55 a.m.

28.3 Experimental Observation and Physics of "Negative" Capacitance and Steeper than 40mV/decade Subthreshold Swing in $Al_{0.83}In_{0.17}N$/AlN/GaN MOS-HEMT on SiC Substrate, H.W. Then, S. Dasgupta, M. Radosavljevic, L. Chow, B. Chu-Kung, G. Dewey, S. Gardner, X. Gao*, J. Kavalieros, N. Mukherjee, M. Metz, M. Oliver*, R. Pillarisetty, V. Rao, S.H. Sung, G. Yang, R. Chau, Intel Corporation, *IQE, Inc.

GaN is a promising material for LED lighting, high voltage power electronics and high power RF applications. GaN HEMT and MOS-HEMT with AlGaN or AlInN polarization layer have been widely studied. In this work we investigate the effects of $Al_{0.83}In_{0.17}N$ polarization layer thickness scaling on the device characteristics of $Al_{0.83}In_{0.17}N$/AlN/GaN MOS-HEMTs on SiC substrates. We have experimentally observed "negative" capacitance and subthreshold swing (SS) steeper than 40 mV/dec in GaN MOS-HEMTs with thin $Al_{0.83}In_{0.17}N$ polarization layer, where composition modulation of Al% and In% dominates.

10:20 a.m.

28.4 Vertical Nanowire InGaAs MOSFETs Fabricated by a Top-down Approach, X. Zhao, J. Lin, C. Heidelberger, E. Fitzgerald, J. del Alamo, MIT

We have demonstrated the first InGaAs GAA NW-MOSFET with a vertical channel fabricated by a top-down approach. Utilizing a novel III-V RIE process and a digital etch technique, we have obtained a peak gm= 730 μS/μm at Vds= 0.5 V, despite a thick EOT=2.2 nm on a device with D=50 nm.

10:45 a.m.

28.5 More than Moore: III-V Devices and Si CMOS Get It Together (Invited), T. Kazior, Raytheon Company

We summarize results on the successful integration of III-V electronic devices with Si CMOS on a common silicon substrate using a fabrication process similar to SiGe BiCMOS. The heterogeneous integration of III-V devices with Si CMOS enables a new class of high performance, 'digitally assisted', mixed signal and RF ICs.

11:10 a.m.
28.6 Dispersion Free Operation in InAlN-Based HEMTs with Ultrathin or No Passivation, R. Wang, G. Li, J. Guo, B. Song, S. Ganguly, B. Sensale-Rodriguez, Z. Hu, Y. Yue, K. Nomoto, F. Faria, J. Verma, S. Rouvimov, X. Gao*, O. Laboutin**, Y. Cao**, W. Johnson**, P. Fay, D. Jena, H.G. Xing, University of Notre Dame, *IQE RF LLC, **IQE KC LLC

The origin and management of DC-RF dispersion in InAlN-based GaN HEMTs is examined, in conjunction with consideration of the implications for device speed. This study in which GaN HEMTs with alloyed and non-alloyed ohmic contacts are compared, renders the following observations and hypotheses: 1) We show that dispersion free operation can be achieved without passivation, which has never been reported before for GaN HEMTs. 2) The root cause of dispersion associated with surface states is often introduced during device processing; in particular, unintentional or unoptimized oxidation of the HEMT surface. 3). These undesired surface states also lead to gate extension (virtual gate), which decreases device speed but increases the breakdown voltage. In addition, the function and efficacy of a plasma based ultrathin passivation is evaluated.

11:35 a.m.
28.7 Depletion-Mode Ga_2O_3 MOSFETs on β-Ga_2O_3 (010) substrates with Si-ion-Implanted Channel and Contacts, M. Higashiwaki, K. Sasaki, M.H. Wong, T. Kamimura, D. Krishnamurthy, Akito Kuramata*, T. Masui**, S. Yamakoshi*, National Institute of Information and Communications Technology, *Tamura Corporation, **Koha Co. Ltd.

We fabricated Ga_2O_3 MOSFETs using Si-ion implantation doping for the channel layer and source/drain electrodes. The MOSFETs exhibited complete channel pinch-off with a breakdown voltage of 415 V and a drain current on/off ratio of 10 orders of magnitude. The devices also showed stable operation up to 250 degrees C.

Session 29: Process and Manufacturing Technology – Advanced BEOL and 3D Integration
Wednesday, December 11, 9:00 a.m.
Columbia Rooms 5&7
Co-Chairs: John Zhu, Qualcomm
Hiroshi Morioka, Fujitsu

9:05 a.m.
29.1 Challenges in Low-k Integration of Advanced Cu BEOL Beyond 14 nm Node (Invited), N. Inoue, Renesas Electronics

Interconnect strategy is considered in the technology and market trends. More capacitive element of FinFET than the conventional planar FET requires lower resistance to the long interconnect, which can be realized by high aspect ratio (AR) wiring. But, high AR wiring degrades the performance in short wiring range due to high capacitance. Then, lowering the k-value is expected to compensate this degradation. Regarding the low-k technology trend, we have issues of PID (plasma-induced damage) and CPI (chip-package interaction) in integration of k~2.5, delaying introduction of much lower k material. High carbon content and enhancing Si-C-Si bridging bond are keys to improve integration performance.

9:30 a.m.

29.2 Superior Cu Fill with Highly Reliable Cu/ULK Integration for 10nm Node and Beyond, T. Matsuda, J. Lee, K. Han, K. Park, J. Cha, J. Baek, T. Yim, D. Kim, D. Lee, I. Kim, B. Kwon, S. Ahn, J. Yun, B. Kim, B. Yoon, N. Lee, S. Choi, H. Kang, E. Chung, Samsung Electronics Co., Ltd.

PVD-TaN/CVD Ru barrier shows its superior Cu gap-fill performance with more than 20% resistance improvement. Its disadvantages including Cu oxide defects and poor TDDB successfully are overcome by stable Cu_2O passivation layer and the hydrophobic robust ULK. Additionally, the optimized Ru condition successfully passes EM criteria. The PVD-TaN/CVD-Ru stack on the robust ULK is a promising candidate for 10nm technology node and beyond.

9:55 a.m.
29.3 Novel Implantation Process of Carbon Nanotubes for Plugs and Vias, and their Integration with Transferred Multilayer Graphene Wires, M. Sato, M. Takahashi, M. Nihei, S. Sato, N. Yokoyama, AIST

We have developed a novel process, implantation of carbon nanotubes (CNTs) into holes like plugs, vias, and TSVs for the first time. This process can densify CNTs compared to directly-grown CNTs. It was found the implanted CNT plugs had a resistance one order of magnitude lower than the directly-grown CNT plugs.

10:20 a.m.
29.4 Applications and Design Styles for 3DIC (Invited), O. Franzon, E. Rotenberg, J. Tuck, W. Davis, H. Zhou, J. Ledford, Z. Zhang, J. Park, B. Dwiel, E. Forbes, J. Hoo, S. Priyardarshi, S. Lipa, T. Thorlofsson*, North Caroloina State University, *Synopsys

The key to gaining substantial benefit from 3DIC technology is to create 3D specific designs that do more than recast a 2D optimal design into the third dimension. This paper explores a number of approaches to creating 3D specific designs. These include previously reported results for memory-on-logic and logic partitioning. We report for the first time a high bandwidth, low latency bus specifically designed to move data in a 3D stack, a 3D processor it enables, and the design of 3D specific communications layers to improve the power efficiency of computing.

10:45 a.m.
29.5 Fabricating 3D Integrated CMOS Devices by Using Wafer Stacking and Via-last TSV Technologies, M. Aoki, F. Furuta, K. Hozawa, Y. Hanaoka, H. Kikuchi*, A. Yanagisawa*, T. Mitsuhashi*, K. Takeda, Hitachi Ltd., *ASET

A three-layer stacked wafer with CMOS devices was demonstrated for the first time by using hybrid wafer bonding and via-last TSV (7 μm diameter/25 μm length) processes. This demonstration confirmed that copper/polymer hybrid wafer bonding brings both seamless copper bonding and void-less underfilling in face-to-face (F2F) and back-to-face (B2F) configurations. Backside via-last TSV processes provide electrical connection between a TSV and copper/low-k interconnects without causing low-k damage. The highest level transmission performance of 15 Tbps/W was achieved by low-capacitance TSV (around 40 fF). Additionally, the estimated keep-out-zone (KOZ) is lower than 2 μm according to ring-oscillator measurements. This remarkably small KOZ is mainly attributed to low residual stress in surrounding silicon (below 50 MPa at 2 μm from the TSV edge).

11:10 a.m.
29.6 Record-High 121/62 μA/μm on-Currents 3D Stacked Epi-Like Si FETs with and without Metal Back Gate, C.-C. Yang, S.-H. Chen, J.-M. Shieh, W.-H. Huang, T.-Y. Hsieh, K.-S. Chang-Liao*,

C. Hu**, F.-L. Yang, National Nano Device Laboratories, *National Tsing HuaUniversity, **University of California, Berkeley

A sequential layered integration technology that can fabricate 3D stackable epi-like Si FETs with and without metal back gate (MBG) under sub-400^{o}C are proposed in this article. With laser crystallized epi-like Si and CMP thinning processes for channel fabrication, 3D stackable ultra thin body (UTB) n/p-MOSFETs with low-subthreshold swing (88 and 121 mV/dec.) and high on-current (121 and 62 uA/um) are demonstrated. With additional metal back gate structure, UTB devices can be desirably operated in a positive or negative threshold voltage range with γ values of 0.51 (n-MOSFETs) and 0.56 (p-MOSFETs) for favoring its applications in 3D logic circuits. In addition, such thin and high quality channel and metal back gate scheme is not only promising for conventional p-n junction device but junctionless (JL) scheme, which can simplify the fabrication and achieve further scaling.

11:35 a.m.
29.7 High Performance Closed-Channel Cooling System Using Multi-channel Electro-osmotic Flow Pumps for 3D-ICs, H. Kudo, Y. Oguri*, A. Tsukune**, Y. Kim**, H. Kitada**, K. Fjimoto, I. Kinefuchi*, Y. Matsumoto, T.Ohba**, Dai Nippon Printing Co., Ltd., *University of Tokyo, **Tokyo Institute of Technology

A multi-channel electro-osmotic flow (EOF) implemented to the closed-channel cooling system (C3S) has been developed for thermal management of stacked chips (3D-ICs). Cooling capability of the EOF pumps fabricated using MEMS technology as high as 140 W/cm2 was demonstrated for the first time.

Session 30: Memory Technology – Conductive Bridge and Phase Change RAM
Wednesday, December 11, 9:00 a.m.
Columbia Rooms 6&8
Co-Chairs: Paul Kirsch, SEMATECH
Yoosang Hwang, Samsung Electronics

9:05 a.m.
30.1 Conductive-Bridge Memory (CBRAM) with Excellent High-Temperature Retention (Invited), J. Jameson, P. Blanchard, C. Cheng, J. Dinh, A. Gallo, V. Gopalakrishnan, C. Gopalan, B. Guichet, S. Hsu, D. Kamalanathan, D. Kim, F. Koushan, M. Kwan, K. Law, D. Lewis, Y. Ma, V. McCaffrey, S. Park, S. Puthenthermadam, E. Runnion, J. Sanchez, J. Shields, K. Tsai, A. Tysdal, D. Wang, R. Williams, M. Kozicki, J. Wang, V. Gopinath, S. Hollmer, M. Van Buskirk, Adesto Technologies Corporation

High-temperature data retention presents a critical hurdle for the emergence of Resistive RAM (RRAM) technologies. We report here on a family of RRAM cells which provide excellent data retention at temperatures exceeding 200ºC, and we discuss the fundamentals of high-T retention in terms of quantum point contacts.

9:30 a.m.
30.2 Investigation of the Physical Mechanisms Governing Data-Retention in Down to 10nm Nano-Trench Al_2O_3/CuTeGe Conductive Bridge RAM (CBRAM), J. Guy, G. Molas, E. Vianello, F. Longnos, S. Blanc, C. Carabasse, M. Bernard, J. F. Nodin, A. Toffoli, J. Cluzel, P. Blaise, P. Dorion, O. Cueto, H. Grampeix, E. Souchier, T. Cabout, P. Brianceau, V. Balan, A. Roule, S. Maitrejean, L. Perniola, B. De Salvo, CEA LETI MINATEC

Conductive Bridging RAM (CBRAM) are envisaged as a promising candidate for future memory generations, due to their high speed, low voltage, low consumption and ease of integration in the back end of a logic process [1-5]. New CBRAM generations use an oxide as electrolyte and a Cu-based active electrode in order to improve the thermal stability (i.e. retention and soldering), tolerating a slight increase of the operating voltages. Nevertheless, an issue of oxide-based CBRAM remains the variability on the HRS (> 1 decade), being at the origin of the dispersion and instability of retention characteristics at high temperature. In this paper, we present Nano-trench TiN/Al_2O_3/CuTeGe based CBRAM offering good scaling capability (down to 10x50nm effective area) and excellent switching control. For the 1st time at our knowledge, the impact of filament morphology, in correlation with the operating conditions, on high temperature retention is addressed.

9:55 a.m.
30.3 Comprehensive Methodology for the Design and Assessment of Crossbar Memory Array with Nonlinear and Asymmetric Selector Devices, A. Chen, GLOBALFOUNDRIES

Technology and design tradeoffs are important for crossbar memory array optimization. A comprehensive model is presented in this paper to assess array functionality with different nonlinear/asymmetric selector parameters, bias schemes, and array designs. Array Vdd should be maximized within power and efficiency constraints. Partial bias schemes can be chosen based on selector types and design targets. Impact of line resistance, contact resistance, and memory variability is analyzed. Parallel access and self-selecting design may improve array performance.

10:20 a.m.
30.4 Interface Engineering for Thermal Disturb Immune Phase Change Memory Technology, A. Redaelli, M. Boniardi, A. Ghetti, U. Russo, C. Cupeta, S. Lavizzari, A. Pirovano, G. Servalli, Micron Semiconductor Italia s.r.l.

The Phase Change Memory (PCM) technology has followed the scaling roadmap from 180nm down to the 45nm technology node. The scaling of a PCM array may give rise to concerns about thermal crosstalk and its reliability implications due to both the temperature driven programming operation and the impact of high temperature on data retention. This issue has been already addressed in 54nm PCM through an accurate tuning of the programming algorithm. Although effective, such an approach implies several constraints for further optimizations of PCM array performances. In this work we empirically investigate the thermal crosstalk in 45nm PCM arrays, clearly showing the key role of the interface thermal resistances. PCM cell design rules for thermal crosstalk immune operation are proposed and validated on silicon, leading to a fully disturb-immune qualified process.

10:45 a.m.
30.5 Charge-Injection Phase Change Memory with High-Quality GeTe/Sb_2Te_3 Superlattice Featuring 70-µA RESET, 10-ns SET and 100M Endurance Cycles Operations, T. Ohyanagi, N. Takaura, M. Tai, M. Kitamura, M. Kinoshita, K. Akita, T. Morikawa, S. Kato*, M. Araidai*, K. Kamiya*, T. Yamamoto*, K. Shiraishi*, LEAP, *University of Tsukuba

A high quality charge-injection GeTe/Sb_2Te_3 superlattice PCM was developed. It showed a RESET-current of 70-µA and a SET-speed of 10 ns, the fastest ever reported. TEM analysis demonstrated the superlattice structure was maintained after 1M endurance. Even 100M endurance was possible and these results conclusively proved non-melting resistive switching.

11:10 a.m.
30.6 Atomic-level Engineering of Phase Change Material for Novel Fast-switching and High-Endurance PCM for Storage Class Memory Application, H.Y. Cheng, M. BrightSky*, S. Raoux*,

C.F. Chen, P.Y. Du, J.Y. Wu, Y.Y. Lin, T.H. Hsu, Y. Zhu*, S. Kim*, H.L. Lung, C. Lam*, Macronix International Co., Ltd., **IBM T. J. Watson Research Center

Storage class memory (SCM) does not need long data retention (since the data are refreshed regularly) but has very stringent requirements on read/write speed and cycling endurance. Although phase change memory (PCM) is a leading candidate but currently no phase change material can satisfy both speed and endurance requirements. This is because although GST-225 is a fast switching material it suffers large volume change when melting thus limited cycling endurance. Attempts to improve the endurance so far must sacrifice switching speed. This work explores new phase change material by atomic-level engineering the doping to GST. The resulting new phase-change material has demonstrated fast switching speed of 20 ns, long endurance of 1G cycles and low reset current of 150 μA in a 128 Mb test chip. Its data retention passed 20 years-55 ^{o}C criteria with failure rate lower than 10ppm.

11:35 a.m.
30.7 A Phase Change Memory Cell with Metallic Surfactant Layer as a Resistance Drift Stabilizer, S. Kim, N. Sosa, M. BrightSky, D. Mori*, W. Kim, Y. Zhu, K. Suu*, C. Lam, IBM T. J. Watson Research Center, *ULVAC, Inc.

We demonstrate a novel confined PCM cell which utilizes a metallic surfactant layer to stabilize the resistance drift in MLC PCM technology. The surfactant layer provides an alternative conductive path to the amorphous region, which makes the cell characteristics immune to amorphous region instabilities such as time-dependent resistance drift.

Entrepreneurs Lunch at IEDM

Sponsored by IEDM and EDS Women in Engineering

Speaker: Steve Nasiri, Nasiri Ventures LLC, Nasiri Foundations

Wednesday, December 11
12:30 pm - 1:30 pm.
Jefferson Room

Speaker: Steve Nasiri, Nasiri Ventures LLC, Nasiri Foundations

Over the past 35 years, Mr. Nasiri has been a serial entrepreneur in Silicon Valley. His most recent and successful venture was InvenSense, which he founded in 2003 and served as the President, Chief Executive Officer and Chairmen since its inception until October of 2012. Under his leadership, the company became the pioneer and global market leader in motion processing solutions for motion-based user interfaces in consumer electronic including smartphones, tablets, game consoles, wearable electronics, and more.

In November 2011, Mr. Nasiri took the company through the initial public offering (IPO), listed on the New York Stock Exchange (NYSE) under the symbol INVN.

Prior to founding InvenSense, Mr. Nasiri held various key positions as a co-founder and or executive of several pioneering startup companies, including SenSym (acquired by Honeywell), NovaSensor (acquired by General Electric), Integrated Sensor Solutions (acquired by Texas Instruments), ISS-Nagano GmbH, Intelligent Sensing Solutions (acquired by Maxim Integrated), and Transparent Optical Networks.

Mr. Nasiri has been the inventor and co-inventor in over 80 patents and patent applications, and has authored many papers and articles in MEMS and consumer electronics.

In 2010, he was selected by Ernst & Young as Entrepreneur of the year for Northern California and in 2013 he was given Alumni Awards of Distinction by San Jose State University.

Session 31: Characterization, Reliability, and Yield – Device Variation and Noise
Wednesday, December 11, 1:30 p.m.
Lincoln Room
Co-Chairs: *Jian Zhang, Liverpool John Moores University*
Yuichiro Mitani, Toshiba Corp.

1:35 p.m.
31.1 Technology Downscaling Worsening Radiation Effects in Bulk: SOI to the Rescue (Invited), P. Roche, J.-L. Autran*, G. Gasiot, D. Munteanu*, STMicroelectronics, *Aix-Marseille Universiy & CNRS, IM2NP

Extrinsic atmospheric radiations are today as important to IC reliability as intrinsic failure modes. More and more industry segments are impacted. Sub-40nm downscaling has a profound impact on the Soft Error Rate (SER) of BULK technologies. The enhanced resilience of latest SOI technologies will fortunately help leveraging existing robust design solutions. Extrinsic atmospheric radiations are today as important to IC reliability as intrinsic failure modes. More and more industry segments are impacted. Sub-40nm downscaling has a profound impact on the Soft Error Rate (SER) of BULK technologies. The enhanced resilience of latest SOI technologies will fortunately help leveraging existing robust design solutions.

2:00 p.m.
31.2 Gate Current Variation: A New Theory and Practice on Investigating the Off-State Leakage of Trigate MOSFETs and the Power Dissipation of SRAM, E.R. Hsieh, S.T. Lin, S. Chung, R.M. Huang*, C.T. Tsai*, L.T. Jung*, National Chiao Tung University, *UMC

A new gate current variation(σI_g) has been proposed for the first time and demonstrated on the trigate devices. It was found that gate current variation can serve as an indicator of the gate sidewall surface roughness. A theory has then been developed and verified experimentally on a trigate with various fin heights. Results show that surface roughness increases with the fin height. Moreover, hot carrier and NBT stresses have also been performed for trigate CMOS FETs. It was found that NBTI exhibits the worst variation. Finally, this theory has been tested on the SRAM to examine the standby power dissipation. Results show that the power dissipation is dominated by the pFET NBTI effect.

2:25 p.m.
31.3 Key Issues and Techniques for Characterizing Time-dependent Device-to-Device Variation of SRAM, M. Duan, J. Zhang, Z. Ji, J. Ma, W. Zhang, B. Kaczer*, T. Schram*, R. Ritzenthaler*, G. Groeseneken*, A. Asenov**, Liverpool John Moores University, *IMEC, **University of Glasgow

Discreteness of aging-induced charges causes a Time-dependent Device-to-Device Variation (TDDV) and SRAM is vulnerable to it. This work analyses the shortcomings of existing methods and propose a new technique. The key issues addressed include the SRAM-relevant sensing Vg, timing, capturing maximum degradation, sampling rate, time window, and test device numbers.

2:50 p.m.
31.4 New Observations on Complex RTN in Scaled High-κ/Metal-Gate MOSFETs - the Role of Defect Coupling Under DC/AC Condition, P. Ren, P. Hao, C. Liu, R. Wang, X. Jiang, Y. Qiu, R. Huang, S. Guo, M. Luo, M. Li, J. Wang*, J. Wu*, J. Liu*, W. Bu*, W. Wong*, S. Yu*, H. Wu*, S.-W. Lee*, Y. Wang, Peking University, *SMIC

The coupling effect between multi-traps in complex RTN is experimentally studied in scaled high-k/metal-gate MOSFETs for the first time. By using extended STR method, the narrow "test window" of complex RTN is successfully expanded to full VG swing. Evident defect coupling can be observed in both RTN amplitude and time constants. Interesting nonmonotonic bias-dependence of defect coupling is found, which is due to two competitive mechanisms of Coulomb repulsion and channel percolation conduction. The decreased defect coupling is observed with increasing AC frequency. Based on the new observations on complex RTN, its impacts on the circuit stability is also evaluated, which shows an underestimation of the transient performance if not considering defect coupling. The results are helpful for future robust circuit design against RTN.

3:15 p.m.
31.5 Understanding Switching Variability and Random Telegraph Noise in Resistive RAM, S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni*, N. Ramaswamy*, D. Ielmini, Politecnico di Milano, *Micron, R&D Unit

Switching variability and noise are among the most critical issues for resistive switching memory (RRAM). Understanding the statistics of ion/electron transport in the conductive filament (CF) is essential to improve and scale RRAM. We addressed switching and read noise in RRAM. We present an analytical model for variability of resistance and switching voltage. Random telegraph noise (RTN) is explained by trap-induced depletion accounting for size-dependent RTN. Bias-dependent RTN is explained by Poole-Frenkel transport and Joule heating in atomic-size CFs.

3:40 p.m.
31.6 Analysis of DC/Transient Current and RTN Behaviors Related to Traps in p-GaN Gate HEMT, J.-H. Bae, S. Hwang*, J. Shin, H.I. Kwon**, C.H. Park***, H. Choi*, J.-B. Park*, J. Kim*, J. Ha*, K. Park*, J. Oh*, J. Shin*, U-I. Chung*, K.-S. Seo, J.-H. Lee, Seoul National University, *Samsung Advanced Institute of Technology, **Chung-Ang University, ***Kwangwoon University

Trap-related transient characteristics and RTN in p-GaN gate HEMT were characterized, for the first time to our knowledge. First current conduction mechanisms in DC I_G is explained based on proposed model. Hopping conduction mechanism is responsible for I_G at $V_G < 0$. I_G at $V_G > 0$ seems to be controlled by thermionic emission and a kind of floating-base n(W)-p(p-GaN)-n(AlGaN/GaN) bipolar transistor. Transient current behavior is related to the DC conduction mechanism and could be explained by thermal emission and charge trapping in p-GaN and AlGaN layers. Measured transient behavior of the CG corresponds to that of the transient currents. Hole trapping into the AlGaN layer is verified by analyzing RTNs in I_G and I_D. Position and activation energy regarding RTN in the HEMT are firstly extracted. RTN time constants are similar to those in I_G and I_D transient behavior.

Session 32: Modeling and Simulation – Modeling Beyond CMOS Devices, Interconnects and GaN HEMT
Wednesday, December 11, 1:30 p.m.
Columbia Rooms 5&7
Co-Chairs: Jing Guo, University of Florida
M.M. De Souza, University of Sheffield

1:35 p.m.
32.1 Self-Heating Effects in Ultra-Scaled Si Nanowire Transistors, R. Rhyner, M. Luisier, ETH Zurich

The goal of this paper is to investigate self-heating effects and local temperature increases in ultra-scaled Si nanowire transistors (NWFET). An electron and phonon quantum transport approach based on the

Non-equilibrium Green's Function formalism is used for that purpose. It ensures current and energy conservation. All the simulations are performed at room temperature. As main results, it is found that the ON-current of NWFETs with a diameter of 3 nm decreases by about 30% due to self-heating and their lattice temperature can reach values up to 500 K on the drain side.

2:00 p.m.
32.2 Are Carbon Nanotubes Still a Viable Option for ITRS 2024?, P. Pillai, P. Umari*, M. De Souza, University of Sheffield, *Università degli Studi di Padova

A critical assessment of the influence of band gap calculated the via the most accurate theoretical approach the "GW approximation" on the performance of CNT-TFETs reveals smaller on-off ratios and on-current than previously estimated using their conventional tight binding band gaps. The revised band gaps are shown to now explain a wide range of experimental devices in the literature. A semiconducting CNT of diameter 0.78nm is the most likely candidate to meet future ITRS targets.

2:25 p.m.
32.3 Modeling of Electron Transport in Biomolecules: Applications to DNA (Invited), M. Anantram, J. Qi, University of Washington

We discuss large scale computational models for electron transport in DNA that can be applied to both electrical methods for sequencing and disease detection. Our models show that decoherence is essential to explain recent experiments. Experimental trends in both length and sequence dependence are captured.

2:50 p.m.
32.4 Simulation of Enhanced Hole Ballistic Velocity in Asymmetrically Strained Germanium Nanowire Trigate p-MOSFETs, J. Teherani, W. Chern, D. Antoniadis J. Hoyt, MIT

The impact of large, asymmetric strain in Ge nanowire (NW) trigate p-MOSFETs with record measured hole mobility is simulated. Hole ballistic velocity enhancement of 2.8X relative to unstrained Si (1.6X relative to 1% strained Si) is predicted for 10-nm wide s-Ge NWs suggesting a scalable enhancement technique for future nodes.

3:15 p.m.
32.5 Is Sub-10nm Thick 3D-Topological Insulator Good for the Local Electrical Interconnects?, G. Gupta, M.B.A. Jalil, G. Liang, National University of Singapore

On examining the feasibility of sub-10 nm thick 3D-TI (Bi_2Se_3) wire for the local electrical interconnects in the presence of edge roughness, vacancies, charge impurities and acoustic phonons across temperature and Fermi-level, we found that because of phonons it may not be the promising material to replace Cu for interconnects.

3:40 p.m.
32.6 Exploring the Design of Ultra-Low Energy Global Interconnects Based on Spin Torque Switches, M. Sharad, X. Fong, K. Roy, Purdue University

Application of low-voltage current-mode spintronic switches in the design of ultra-low energy and high-performance global on-chip interconnects is proposed and analyzed. Simulations show the possibility of achieving ~100x low-energy as compared to conventional CMOS techniques. A case study for on-chip MRAM cache simulation shows over ~90% reduction in energy for on-chip memory access, using the proposed interconnect design.

4:05 p.m.
32.7 High Voltage GaN HEMTs Compact Model: Experimental Verification, Field Plate Optimization and Charge Trapping, U. Radhakrishna, D. Piedra, Y. Zhang, T. Palacios, D. Antoniadis, MIT

High voltage GaN HEMTs are leading contenders for power conversion and switching applications [1]. An accurate physics-based compact device model for this emerging technology is essential for device and circuit design. Several GaN HEMT compact models have been discussed but are not physics-based [2]-[3]. Here, a new physics-based compact model for HV-GaN HEMTs, the MIT Virtual Source GaNFET-High Voltage model (MVS-G-HV) is proposed. The model is geometry scalable and captures static and dynamic device behavior through self-consistent current and charge expressions. The access regions, which are important in device linearity [4] and reverse voltage blocking, are modeled as implicit-gated transistors. The model includes the effect of field plates and can be used to maximize the BV2 Gon figure-of-merit. In addition, 'knee-walkout' in these devices is captured in the model through a simple trap-transistor model. The model requires a small number of parameters with straightforward physical meanings and is validated against DC–IV, S-parameter, breakdown and pulsed measurements of fabricated devices.

Session 33: Circuit and Device Interaction – Circuit/Device Variability and Reliability
Wednesday, December 11, 1:30 p.m.
Columbia Rooms 6&8
Co-Chairs: Shaofeng Yu, SMIC
Francois Andrieu, CEA/LETI

1:35 p.m.
33.1 Simulation Based Transistor-SRAM Co-Design in the Presence of Statistical Variability and Reliability (Invited), A. Asenov, B. Cheng, X. Wang, A. Brown*, D. Reid*, C. Millar*, C. Alexander*, J. Kuang**, S. Nassif**, University of Glasgow, *Gold Standard Simulations, Ltd., **IBM

We report a systematic simulation study of the impact of process and statistical variability and reliability on SRAM cell design in a 14nm technology node SOI FinFET transistors. A comprehensive statistical compact modelling strategy is developed for early delivery of a reliable PDK, which enables TCAD-based transistor-SRAM co-design and path finding for emerging technology nodes.

2:00 p.m.
33.2 Suppression of Die-to-Die Delay Variability of Silicon on Thin Buried Oxide (SOTB) CMOS Circuits by Balanced P/N Drivability Control with Back-Bias for Ultralow-Voltage (0.4 V) Operation, H.Makiyama, Y. Yamamoto, H. Shinohara, T. Iwamatsu, H. Oda, N. Sugii, K. Ishibashi*, T. Mizutani**, T. Hiramoto**, Y. Yamaguchi, LEAP, *The University of Electro-Communications, *The University of Tokyo

Small-variability transistors such as silicon on thin buried oxide (SOTB) are effective for reducing the operation voltage (V_{dd}). This paper proposes the balanced n/p drivability for reducing the die-to-die delay variation by back bias for various circuits. Excellent variability reduction by this balanced control is demonstrated at V_{dd} = 0.4 V.

2:25 p.m.
33.3 Analysis of Transistor Characteristics in Distribution Tails beyond ±5.4σ of 11 Billion Transistors, T. Mizutani, A. Kumar, T. Hiramoto, The University of Tokyo

Transistors in distribution tails of 11G (11 billion) transistors were intensively measured and compared with transistors in the center of distribution. It is found that extrapolated V_{TH} (V_{THEX}) roughly follows the normal distribution, while some transistors show extraordinary small on-current (I_{ON}) which deviates from the normal distribution. The origin of abnormal distribution and the impact on yield loss are discussed.

2:50 p.m.
33.4 Energy Efficiency Comparison of Nanowire Heterojunction TFET and Si MOSFET at Lg=13nm, Including P-TFET and Variation Considerations, U. Avci, D. Morris, S. Hasan*, R. Kotlyar*, R. Kim, R. Rios, D. Nikonov, I. Young, Design and Technology Solutions, *Intel Corp.

Reducing supply voltage (V_{dd}) while keeping leakage current low is critical for minimizing energy consumption and improving mobile device battery life. A Tunneling Field Effect Transistor (TFET) is not limited by subthreshold thermal tail and may perform better than CMOS at low V_{dd}. In this paper, a leading N-TFET option -GaSb/InAs heterojunction- is atomistically modeled and circuit simulation models are developed. Het-j TFET logic with symmetric N- and P-TFET transistors is expected to have 64% energy savings compared to CMOS for low-power applications at Lg=13nm (i.e. 2018 ITRS node). Both MOSFET and TFET device variations are dominated by work-function variation and energy savings are slightly lowered when variations are considered. Without a good pull-up transistor option, energy efficiency is reduced greatly, highlighting the need for exploration of a steeper SS P-TFET to realize significantly superior power efficiency from TFET logic circuits.

3:15 p.m.
33.5 A Unified Approach for Trap-Aware Device/Circuit Co-Design in Nanoscale CMOS Technology, R.Wang, M. Luo, S. Guo, R. Huang, C. Liu, J. Zou, J. Wang*, J. Wu*, N. Xu**, W. Wong*, S.Yu*, H. Wu*, S.-W. Lee, Y. Wang, Peking University, *SMIC, **University of California, Berkeley

In this paper, the major physical effects caused by gate oxide traps in MOSFETs have been integrated for the first time by a proposed unified approach in realistic manners based on industry-standard EDA tools, aiming at practical trap-aware device/circuit co-design. The recently-found AC or transient effects of traps and the interplays with manufacturing process variations are included, with demonstrations on two representatives (RO and SRAM) under realistic digital circuit operations. The proposed approach and the results are helpful for robust and resilient device/circuit co-design in future nano CMOS technology.

3:40 p.m.
33.6 A Novel Physics-Based Variable NBTI Simulation Framework from Small Area Devices to 6T-SRAM, T. Naphade, K. Roy*, S. Mahapatra, Indian Institute of Technology Bombay, *Purdue University

A novel, integrated framework is developed to simulate physics-based variable NBTI in devices and study its impact on circuits. Device-level NBTI variability is simulated by integrating 3D stochastic Reaction-Diffusion model for interface trapping and Two Well model for hole trapping with 3D TCAD for time-zero variability and electrostatics. Time evolution of distributions of interface trap density, hole trap density and resulting V_T shift and V_T are simulated for stress and recovery. Exponential distribution of single-charge impact on V_T shift is verified using TCAD. Simulated V_T shift distribution matches well with experiments, analytic models, and shows correlation between mean and variance. Kolmogorov Smirnov test verifies the simulated V_T shift (Gamma) and V_T (Gaussian) distributions. NBTI variability of different 6T-SRAM metrics are obtained and correlated to device V_T variability.