High-Performance Analog and RF Circuit Simulation using the Analog FastSPICE™ Platform at Columbia University

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1 Introduction

The research group led by Professor Peter Kinget at the Columbia University Integrated Systems Laboratory (CISL) focuses on cutting edge analog and RF circuit design using digital nanoscale CMOS processes. Areas of research include design techniques for circuits operating below 1 V, digitally calibrated RF front ends for superior linearity performance, LO synthesizers for wireless applications, and low-power data converters. Key challenges in the design of these circuits include block-level characterization and full-circuit verification. This paper highlights these verification challenges by discussing the results of a 2.2 GHz PLL LC-VCO, a 12-bit pipeline ADC, and an ultra-wideband transceiver, and the benefits of using the Analog FastSPICE (AFS) Platform from Berkeley Design Automation for nanometer circuit verification [1].

2 Verification Challenges

Verification of innovative circuit designs in an academic environment involves several challenges. Similar to the industrial environment, aggressive schedules are common, driven by competition in demonstrating novel circuits and systems, foundry slot availability, and project budgets. The projects are typically managed by one person who is responsible for the entire system architecture as well as for the detailed design of a large number of subsystems. Comprehensive verification and analysis of individual blocks frequently becomes the bottleneck in determining achievable specifications, which in turn delays the process of system architecture. Circuit simulation times are lengthy primarily due to the following conditions:

1. The circuit has a large element count.
2. The ratio of time constants (μs) to simulation time steps (ps) is large.
3. A strict tolerance setting (such as reltol = 10^{-4} or 10^{-5}) is necessary to achieve the required accuracy.

A nanometer SPICE-accurate simulator with the best possible performance is required to overcome this verification bottleneck. The Analog FastSPICE Platform from Berkeley Design Automation has enabled CISL to address these circuit verification challenges and shorten the chip design cycle. The remainder of this paper provides verification results for sample analog/RF circuit designs using AFS.

3 LC-VCO for 2.2 GHz Frac-N PLL

Several data transmission and communication applications require low integrated noise PLLs to meet their aggressive jitter and noise specifications. Low integrated noise PLLs are achieved when the PLL loop bandwidth is such that the integrated noise has an equal contribution from the out-of-band noise (dominated by the VCO noise) and the in-band noise (typically dominated by the phase detector noise). Low integrated noise requires both low VCO noise and high-gain phase detectors with low noise [2].

One such PLL application at CISL uses an LC-VCO without tail current, operating at low supply voltage and with no noise contributions due to bias circuits. The VCO uses a 6-bit control for frequency tuning, setting the capacitance of a capacitor bank for coarse frequency tuning and varactors for fine frequency tuning. Figure 1 shows the circuit implementation of the VCO.

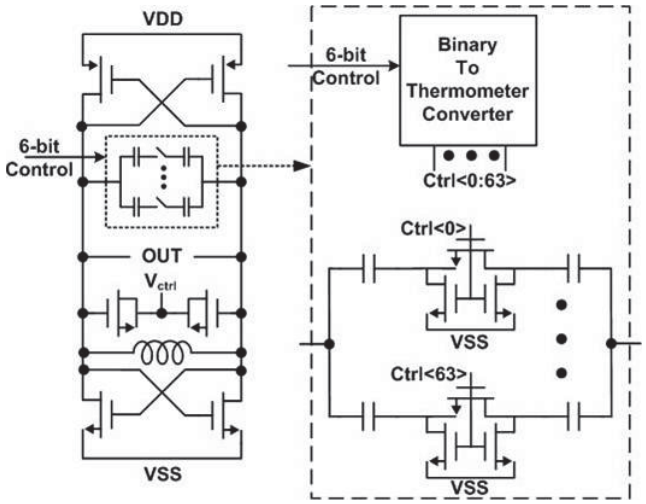

Figure 1 Circuit implementation of the LC-VCO

The VCO consumes 3 mA and was designed to have a gain of 150 MHz/V with a tuning range from 1.9 GHz to 2.3 GHz. The measured phase noise is -112 dBc/Hz at 1 MHz. AFS delivers high-performance and nanometer accurate results for this circuit, as can be seen in Figure 2.

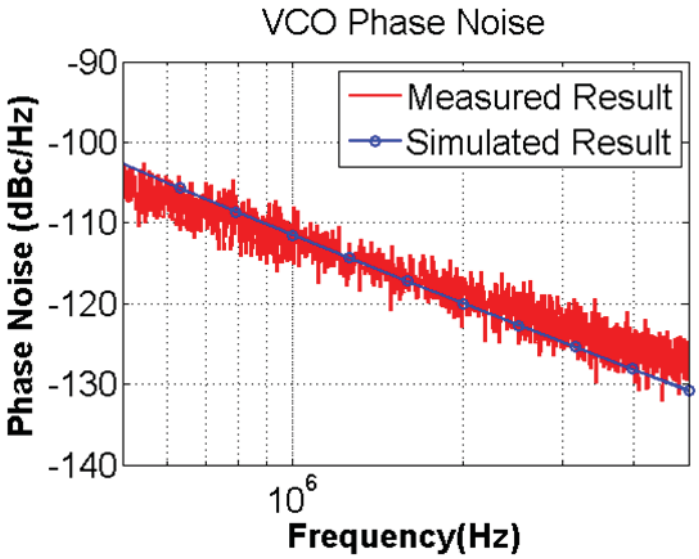

Figure 2: Comparison of simulated to measured phase-noise of the LC-VCO

4 Pipeline ADC

Many communication systems require high-speed medium-resolution analog-to-digital converters (ADCs). These circuits also require low power consumption, small area, and circuit architectures compatible with nanometer digital CMOS processes to achieve the required SoC cost reduction. Pipeline ADCs are widely used in such applications [3].

Targeting such applications, a zero-crossing-based low-power 12-bit Pipeline ADC is being developed at CISL. The expected Signal to Distortion Ratio (SDR) is 75 dB. The simulation time step needs to be in the order of 1ps to accurately simulate the interstage ADC gain, which depends on the time interval for which current sources charge a capacitor. A 256-point FFT is needed to calculate the SDR to this accuracy, translating to a total simulation time of over 5 μs. The large ratio of simulation time to simulation time step significantly increases the verification time.

This circuit has roughly 50 k nodes and 10 k active devices. The biggest challenge in the verification of this circuit is the ability to simulate the complete system. Table 1 shows the results of several simulations, comparing AFS to a traditional SPICE simulator. The values used for `reltol` and simulation `maxstep` were 10^{-4} and 1 ps, respectively.

Table 1: Comparison of pipeline ADC simulation results

First pipeline stage performance verification – schematic netlist		
	AFS	**Traditional SPICE**
Node count	2913	2770
BSIM count	5706	5922
SDR	74 dB	74.5 dB
Simulation run time	4 hr 10 min	20 hr 30 min

Last pipeline stage performance verification – layout extracted netlist		
	AFS	**Traditional SPICE**
Node count	1767	1450
BSIM count	7956	8733
SDR	47.4 dB	47 dB
Simulation run time	2 hr 9 min	10 hr 22 min

Full pipeline circuit functionality verification – schematic netlist		
	AFS	**Traditional SPICE**
Node count	48580	Did not converge
BSIM count	10140	
Simulation run time	7 hr 15 min	

Full pipeline circuit with ESD circuit and packaging parasitics		
	AFS	**Traditional SPICE**
Node count	75543	Did not converge
BSIM count	16709	
Simulation run time	120 hr	

AFS delivered 5x faster simulation than traditional SPICE for the pipeline stage. For the full-circuit simulation, the traditional SPICE simulator aborted after simulating a few hundred picoseconds, while AFS completed all simulations without any issues. In addition, AFS was able to handle the full-circuit verification, including post-layout parasitics, ESD structures, and packaging parasitics. Figure 3 shows the ADC layout.

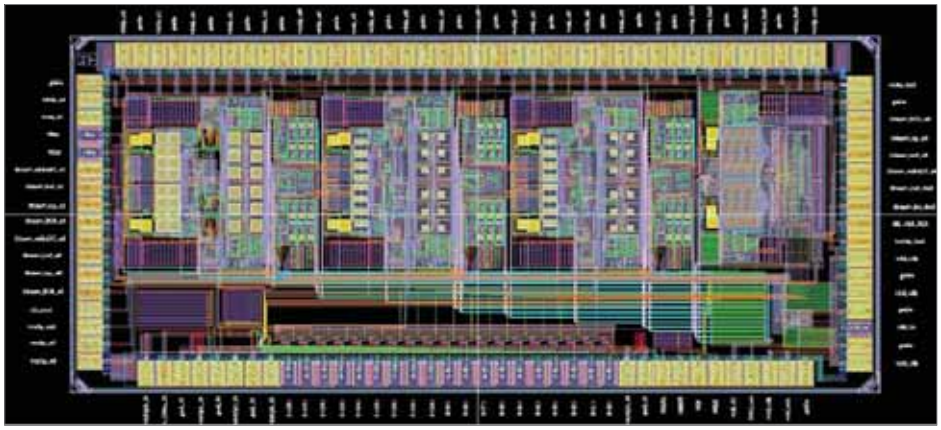

Figure 3: Pipeline ADC chip layout

5 Ultra-Wideband Transceiver

The final example is an ultra-wideband (UWB) Transceiver. UWB is a radio technology that uses short pulses (typically less than 4 ns) with very large signal bandwidths, resulting in average power spectral density (PSD) that is orders of magnitudes lower than that in a carrier-based system. Since 2002, the Federal Communication Commission (FCC) allows UWB transmissions in the 3.1–10.6 GHz range with a bandwidth of at least 500 MHz and a PSD of -41.3 dBm/MHz or less.

UWB is well-suited for short-distance, ultra-low-power wireless communications. The short pulse duration allows transmitters to operate with very low duty cycles and, therefore, very low power consumption. Interest in UWB communications has grown significantly for applications in sensor networks, tag networks, and biomedical applications, where low cost, low power-consumption, and low complexity are highly desirable [4].

Circuit verification for this UWB transceiver needs to include power supply duty cycling, and transient simulation must include noise analysis in order to measure true system performance. The targeted data rate is 1 Mbps, thus simulation time is in the order of microseconds. The carrier frequencies are 3.6 to 4.7 GHz, thus limiting the time steps to less than 1 ps. The circuit contains roughly 6.5 k nodes and 16 k devices. Table 2 shows the transient simulation results, including functionality check, and Figure 4 shows a chip layout of the receiver. AFS was 6x faster than traditional SPICE for this design.

Table 2: Ultra-wideband transceiver simulation results

Ultra-wideband transceiver transient simulation		
	AFS	**Traditional SPICE**
Simulation run time	15 min	1 hr 30 min

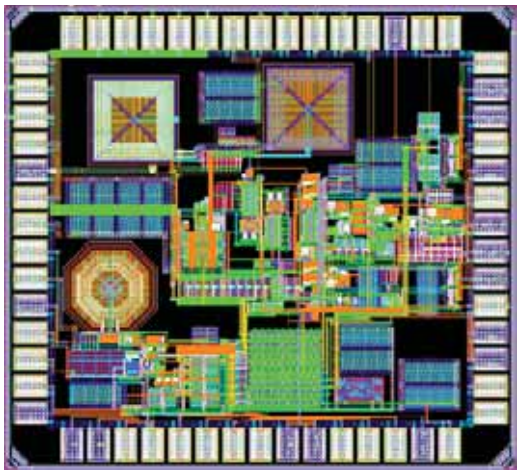

Figure 4: Ultra-wideband transceiver chip layout

6 Conclusion

This paper provides verification results for analog/RF circuits designed by the Columbia University Integrated Systems Laboratory research group, led by Professor Peter Kinget. The circuits presented are an LC-VCO for a 2.2 GHz PLL, a full-circuit pipeline ADC, and a UWB transceiver. These results highlight the differentiation in accuracy, capacity, and performance delivered by the AFS platform. An invaluable tool at Columbia University Integrated Systems Laboratory, AFS enables much higher tape-out confidence and significantly improves research productivity.

7 References

[1] Peter Kinget, Keynote Address, 24th International Conference on VLSI Design at IIT Madras (Chennai, India), “Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply, Reduce the Area and Use Digital Gates,” January 5, 2011.
[2] Chun-wei Hsu, Karthik Tripurari, Shih-An Yu, and Peter R. Kinget, “A 2.2GHz PLL using a Phase-Frequency Detector with an Auxiliary Sub-Sampling Phase Detector for In-Band Noise Suppression,” Proceedings of the 2011 Custom Integrated Circuits Conference.
[3] Junhua Shen and Peter R. Kinget, “Current-Charge-Pump Residue Amplification for Ultra-Low-Power Pipelined ADCs,” IEEE Transactions On Circuits And Systems—II: Express Briefs, Vol. 58, No. 7, July 2011.
[4] Marco Crepaldi, Chen Li, Jorge R. Fernandes, and Peter R. Kinget, “An Ultra-Wideband Impulse-Radio Transceiver Chipset Using Synchronized-OOK Modulation,” IEEE Journal Of Solid-State Circuits, Vol. 46, No. 10, October 2011.