Course Organizer: Yuan Taur, UCSD

In this short course, we invite world's leading experts to give us their vision on what's needed for future CMOS technology to scale to 5 nm and beyond. 5 nm is within a factor of ten of the atomic size, which demands a paradigm shift in many aspects of the technology: device type, process integration, interconnect, patterning, and manufacturability.

For device and material options, III-V MOSFETs, band-to-band tunnel FETs, nanowire FETs, and 2D semiconductors will be considered, among other options. Their merits and challenges, with reference to today's state-of-the-art 14 nm FinFETs, will be discussed. For process integration, the focus is on scaling of fully depleted devices, FinFETs, high-mobility channel material, and SRAM cell. Opportunities include horizontal and vertical nanowires with 3D integration. Interconnects will face power dissipation, insufficient bandwidth, and signal latency problems. The question is how far can we push Cu/low-k to its physical limitation? And will alternative schemes, like carbon nanotubes, optical interconnects, and 3D interconnects meet the challenge? Patterning at 5 nm and beyond will be extremely demanding, requiring a multiplex of resolution enhancing techniques and extreme ultra-violet lithography whose status will be reviewed. Challenges on the resist and mask will also have to be met. Variability is the maker or breaker of CMOS manufacturing at 5 nm. Various sources of local, global, and time dependent variability will be examined. Design-technology co-optimization (DTCO) will be discussed as one of the possible solutions. The short course will conclude with a few thoughts from the organizer on the historical perspective.

Yuan Taur received the Ph.D. degree in physics from University of California, Berkeley, in 1974. From 1981 to 2001, he was with the Silicon Technology Department of IBM Thomas J. Watson Research Center, Yorktown Heights, New York, where he was Manager of Exploratory Devices and Processes. Since 2001, he has been a professor in the Department of Electrical and Computer Engineering, University of California, San Diego. He was appointed a Distinguished Professor in 2014. Dr. Yuan Taur was elected a Fellow of the IEEE in 1998. He has served as Editor-in-Chief of the IEEE Electron Device Letters from 1999 to 2011. Dr. Yuan Taur has authored or co-authored over 200 technical papers and holds 14 U.S. patents. He co-authored a book, "Fundamentals of Modern VLSI Devices," published by Cambridge University Press in 1998. The 2nd edition was published in 2009. Dr. Yuan Taur received IEEE Electron Devices Society's J. J. Ebers Award in 2012 "for contributions to the advancement of several generations of CMOS process technologies." He also received IEEE Electron Devices Society's Distinguished Service Award in 2014.