Conventional memory technologies : DRAM

Instructor: Changyeol Lee, research fellow, SK Hynix

- Current technology
- Further scaling roadmap
- Issues and potential roadblocks
- Including 3D stacked IC

Changyeol Lee

Changyeol Lee received the degree in electronics engineering from Sogang University, Seoul, Korea in 1989, the M.S and Ph.D. degree in electronics engineering from KAIST, Korea, in 1991 and 1997, respectively. His doctorial dissertation studied a short channel SOI device modeling and simulation.

From 1995 he has worked in SK Hynix, Icheon, Korea with joining in more than 20 projects to develop SRAM and DRAM products as a device design and failure analysis engineer and project manager. Currently he is a research fellow in the area of developing reliability model and simulation for DRAM products. He also takes charge of ESD and EOS design and test for DRAM , Flash and Logic IC.